

Compal Confidential

Model Name : Olvia\_BE  
Compal Project Name : A4W1E  
File Name : LA-C801P

# Compal Confidential

## A4W1E Schematics Document

AMD "Beema" Platform

AMD 15W APU With Puma+ Core

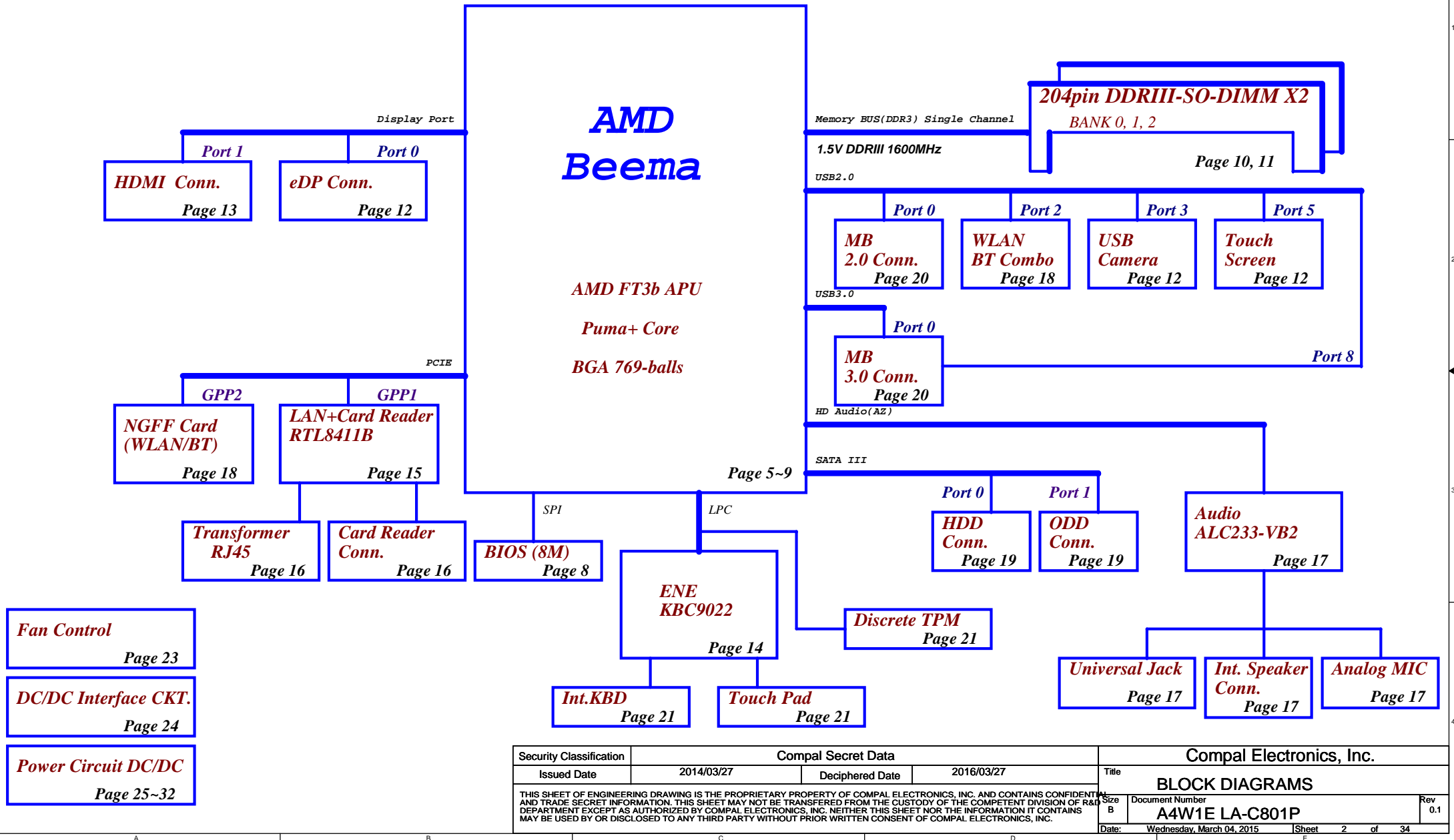
LA-C801P REV: 1.A

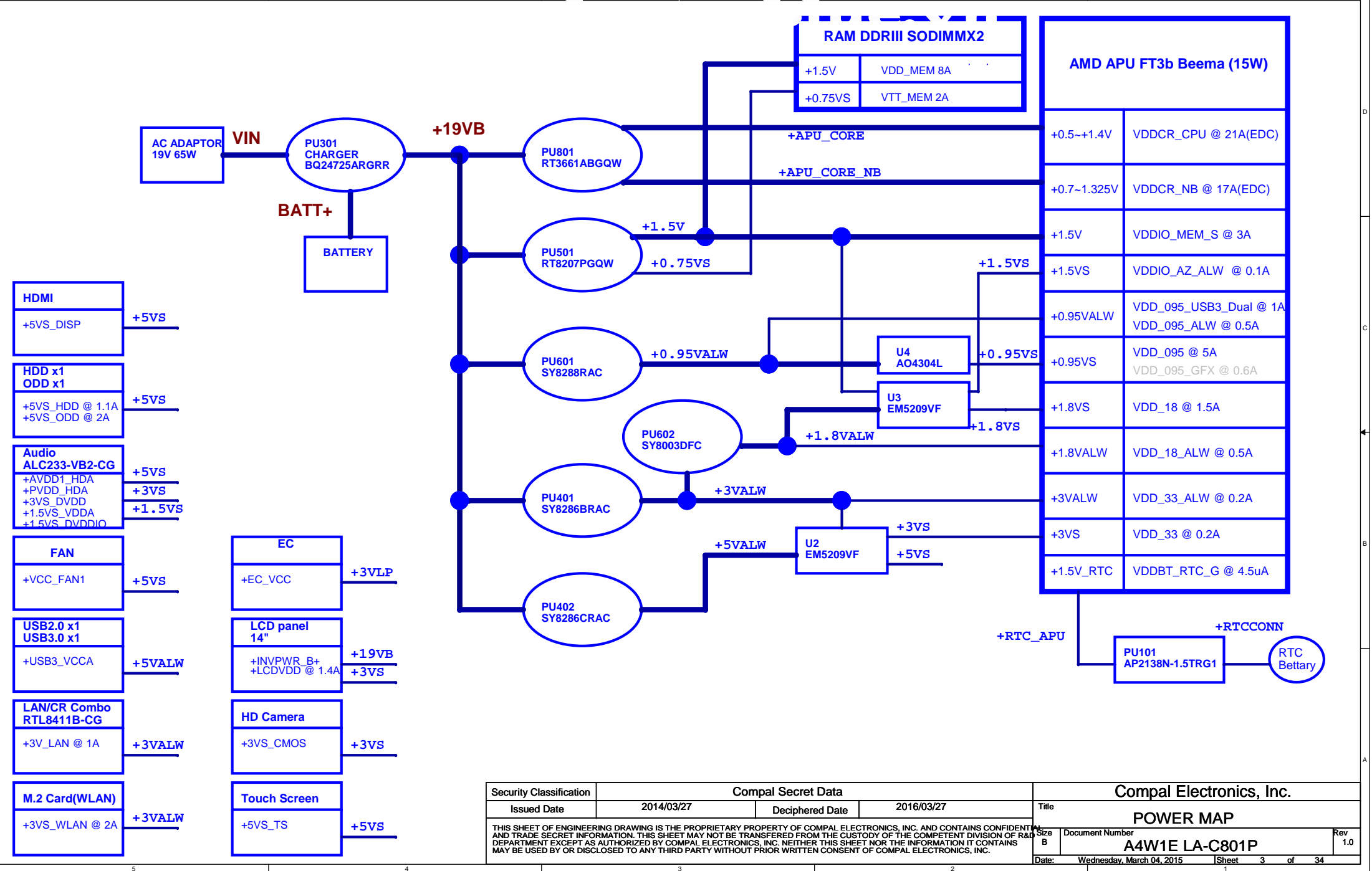
2015-03-30

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				Date	Monday, March 30, 2015	Sheet 1 of 34

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Model Name : A4W1E



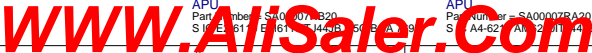


[illegible]

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			



Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
EMC@	EMI pop component
@EMC@	EMI unpop component
JP@	Jump
TP@	Test point
SP@	Short pad for clear CMOS
HDT@	HDT+ for test phase, MP remove
RS@	R-short
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
A8@,A6@,A4@	APU Part Number for A4,A6,A8 APU
E1@,E2@	APU Part Number for E1,E2 APU
BL@	Keyboard backlight
TPM@	Use discrete TPM module
TPUSB@	Use USB to I2C IC for T/P
ECI2C@	Use EC I2C T/P
@RF@	RF unpop component
233@	Use for Audio Codec ALC233-VB2
KBN@	Stuff when use Kabini APU
BMA@	Stuff when use Beema APU
CZL@	Stuff when use Carrizo-L APU
BYOC@	Stuff when support BYOC
NBYOC@	Stuff when non-support BYOC

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1(Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

**G-A** ———— +RTC  
EC\_ON

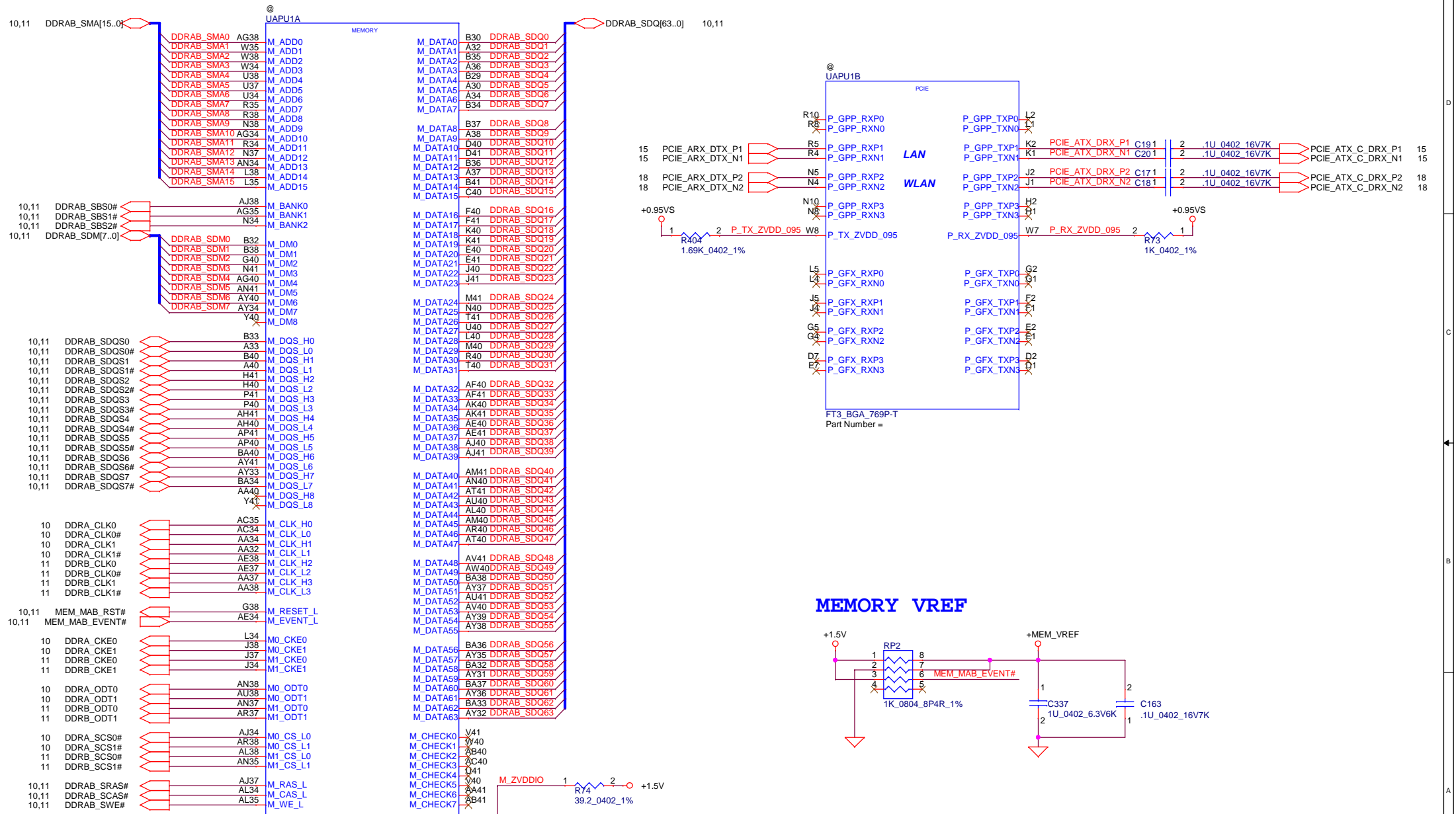
**G-B** ———— +3VALW/+5VALW  
+1.8VALW  
+0.95VALW  
SYSON

**G-C** ———— +1.5V  
SUSP#

**G-D** ———— +3VS  
+1.8VS  
+1.5VS  
+0.95VS  
VR\_ON

**G-E** ———— +APU\_CORE  
+APU\_CORE\_NB

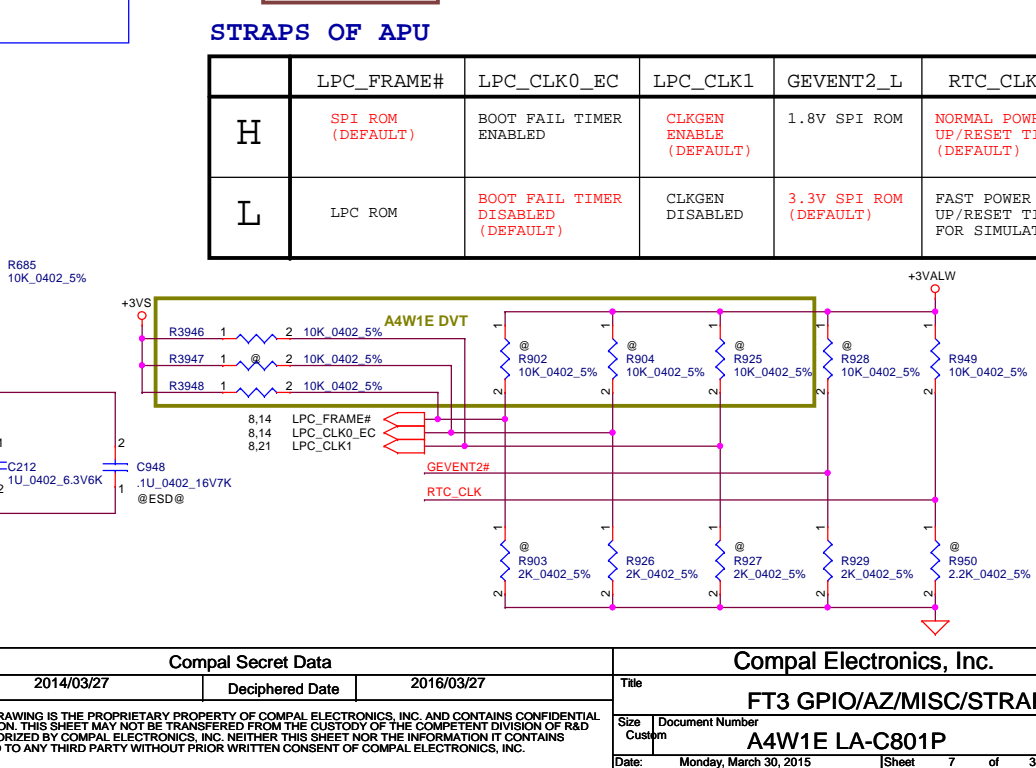
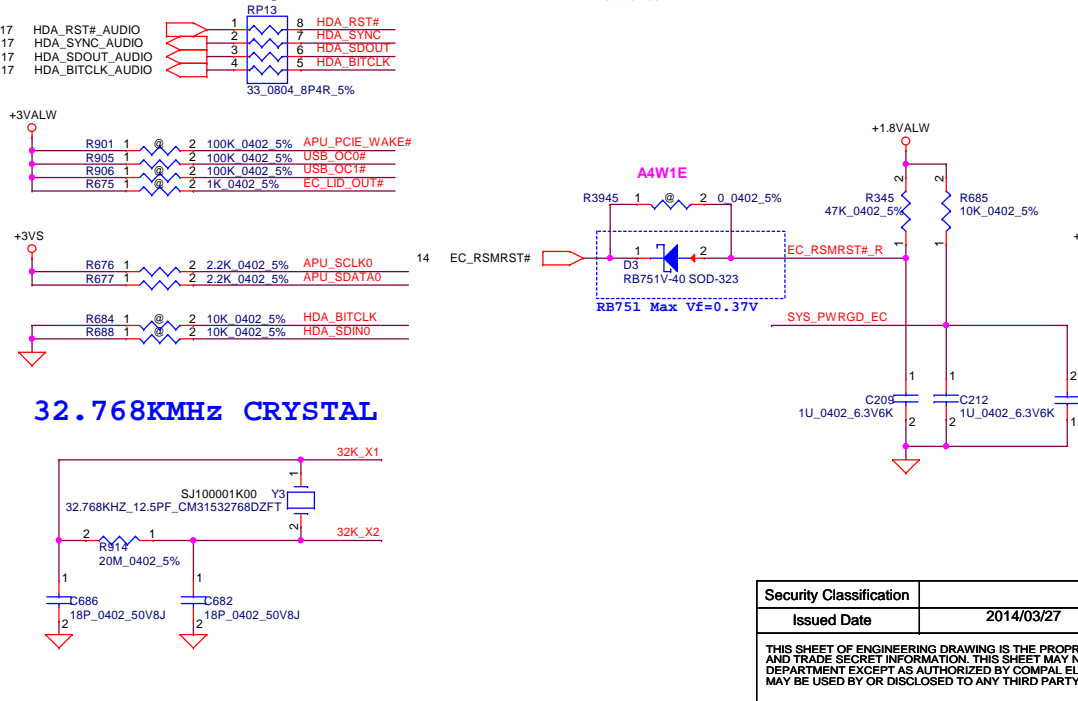
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				Date	Monday, March 30, 2015	Sheet 4 of 34



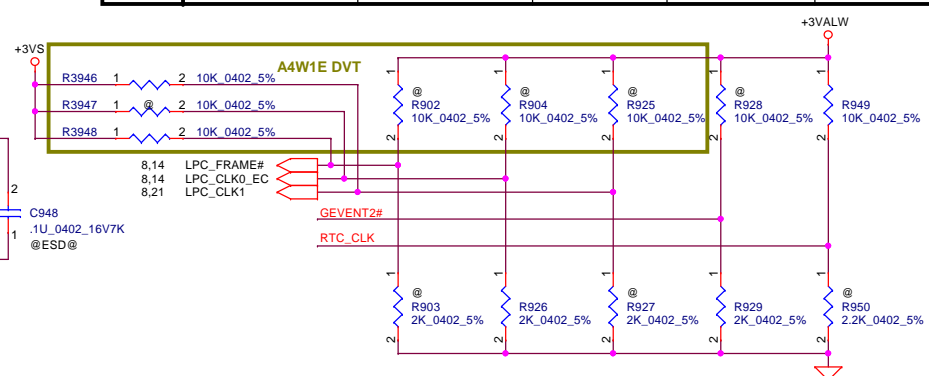
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Document Number		Date		Sheet 5 of 34	
A4W1E LA-C801P		Wednesday, March 04, 2015			



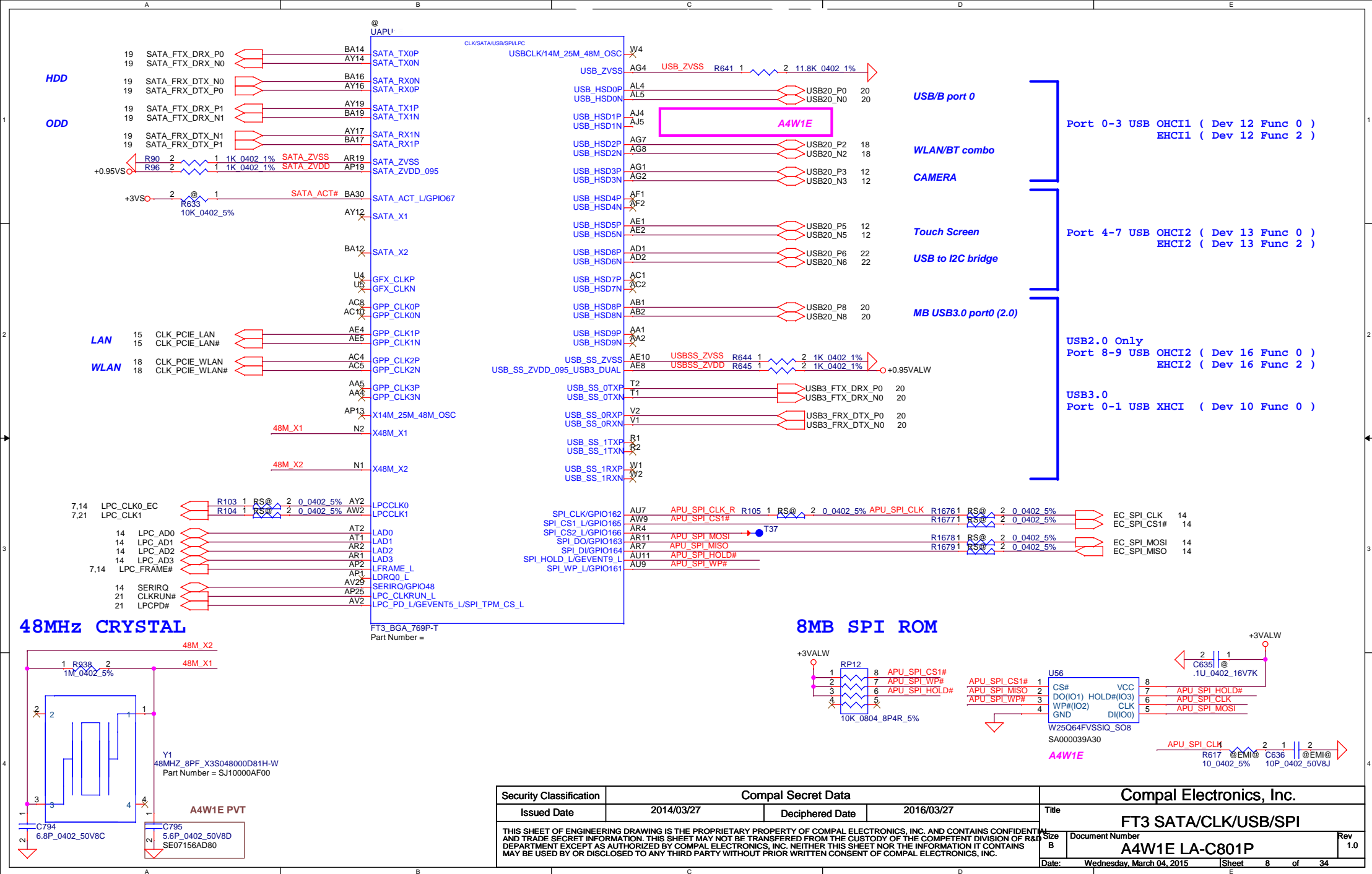




	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMIN (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMIN FOR SIMULATION

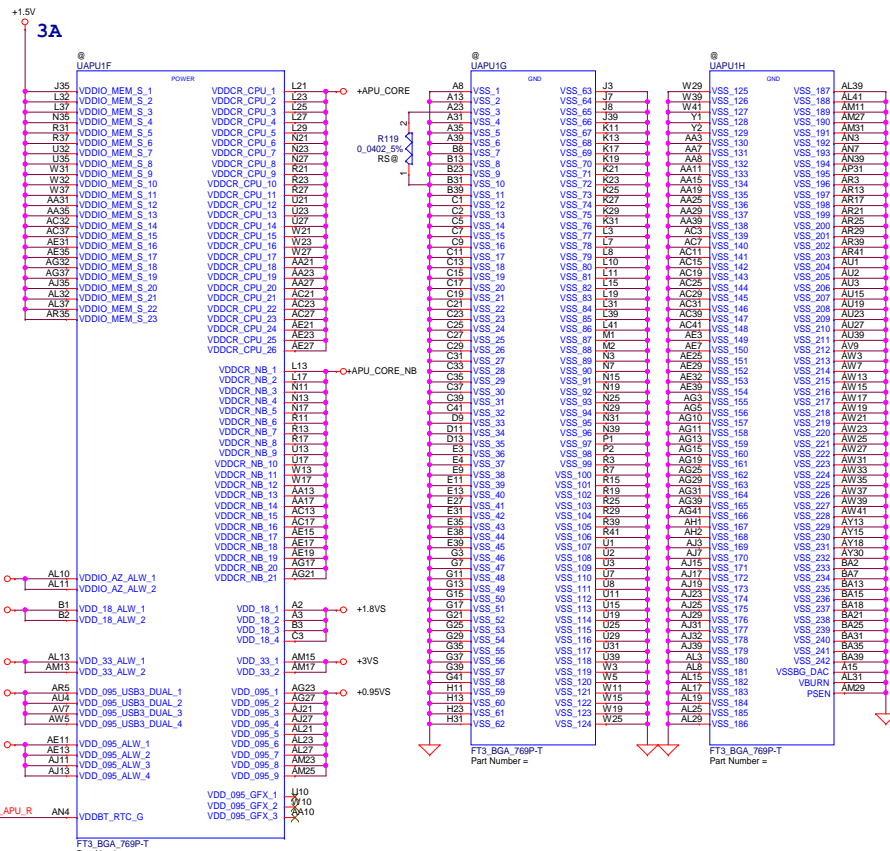


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				Custm	A4W1E LA-C801P	1.0
Date:	Monday, March 30, 2015			Sheet	7	of 34



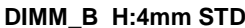


The schematic diagram illustrates the power supply network for the VDDCR\_CPU. It starts with a +APU\_CORE input connected to a network of capacitors (C180 to C195) and inductors (L180 to L195). The capacitors are labeled with values like 1, 2, or 2. The inductors are labeled with values like 1 or 2. The network is connected to a GND symbol.

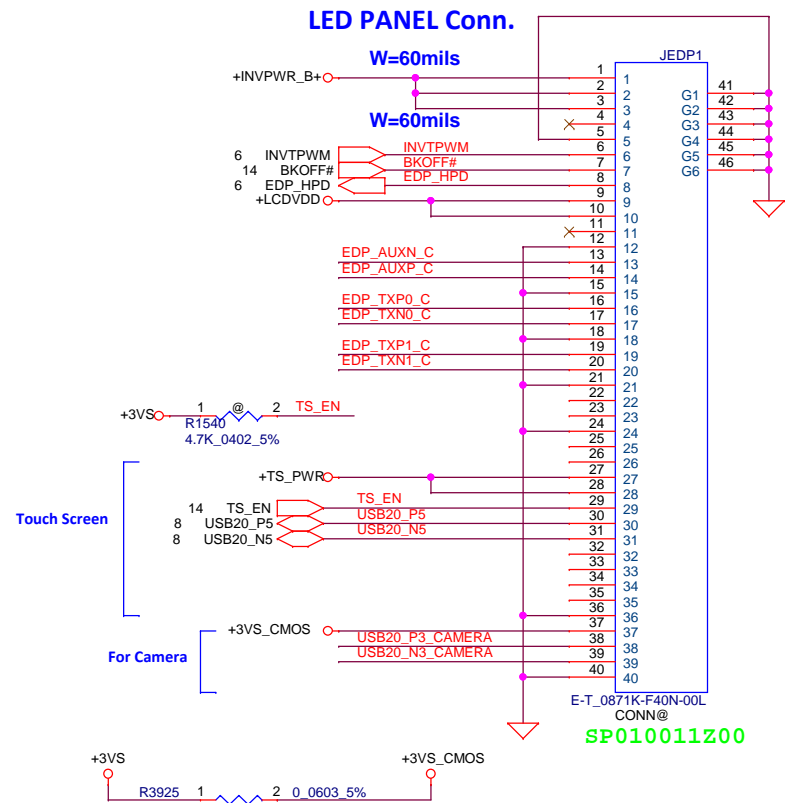
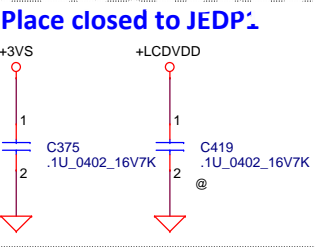
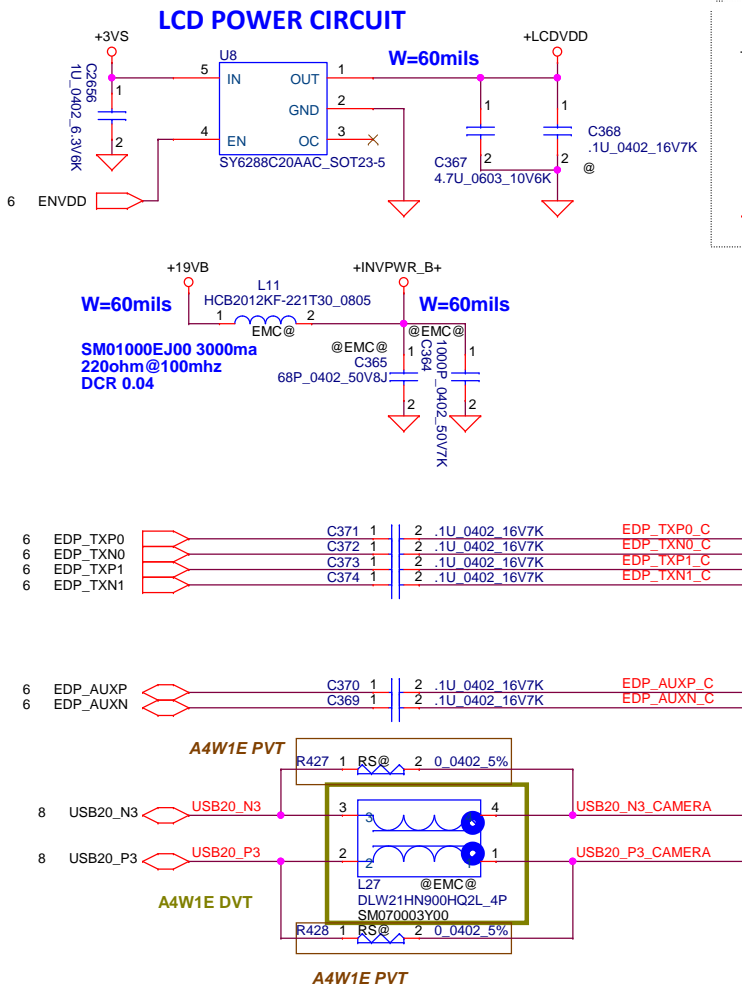
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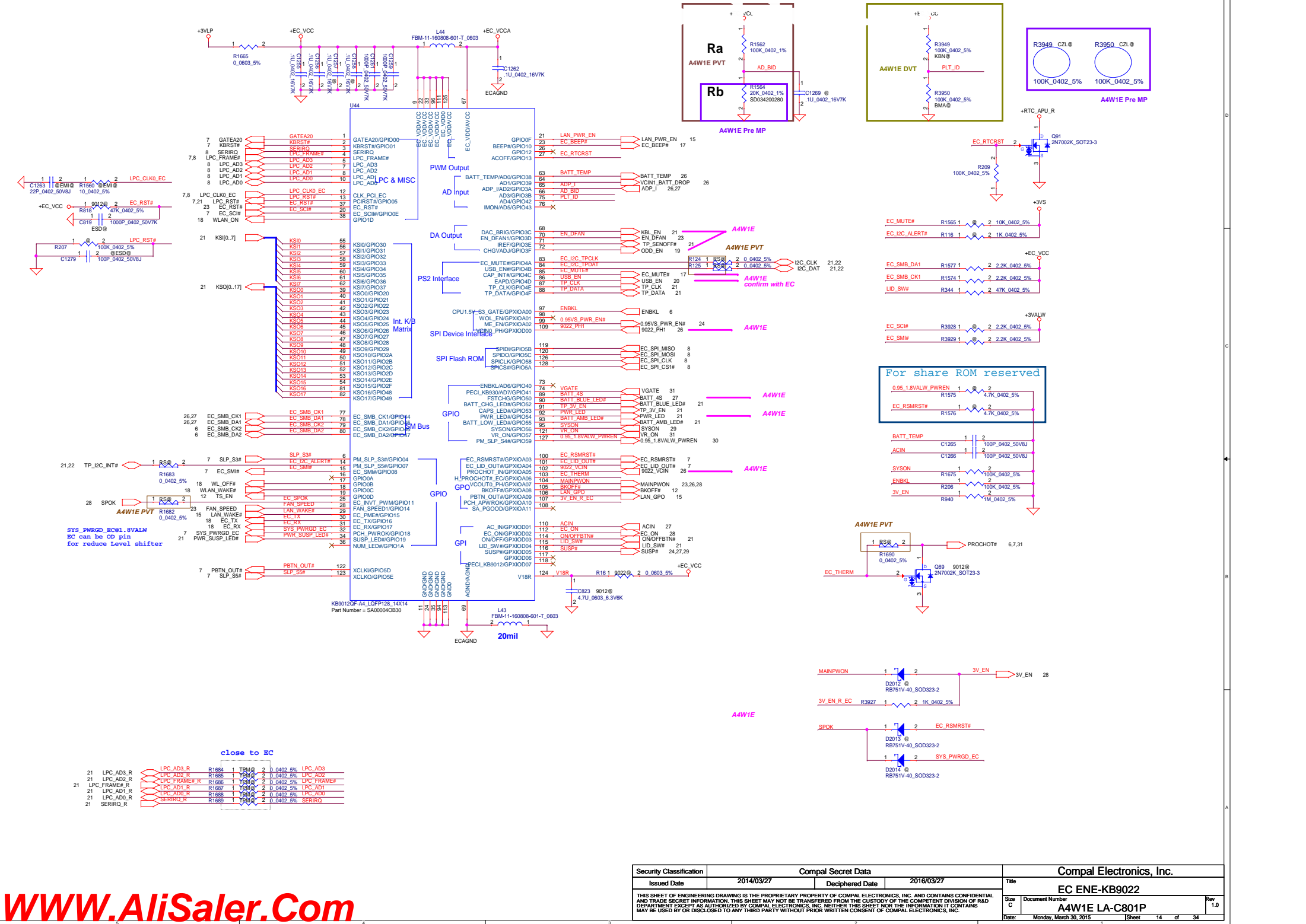


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				A4W1E LA-C801P		
				Date: Wednesday, March 04, 2015	Sheet 11 of 34	



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				A4W1E LA-C801P	0.1
Date: Monday, March 30, 2015				Sheet 12 of 34	





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				EC ENE-KB9022
Size	C	Document Number	A4W1E LA-C801P	Rev 1.0
Date: Monday, March 30, 2015		Sheet 14 of 34		



# LAN-RTL8411B

## From EC

High active.

EN threshold voltage min:1.2V typ:1.6V max:2.0V

Current limit threshold 1.5\*2.8A

+3V\_LAN Rising time must >0.5ms and <100ms

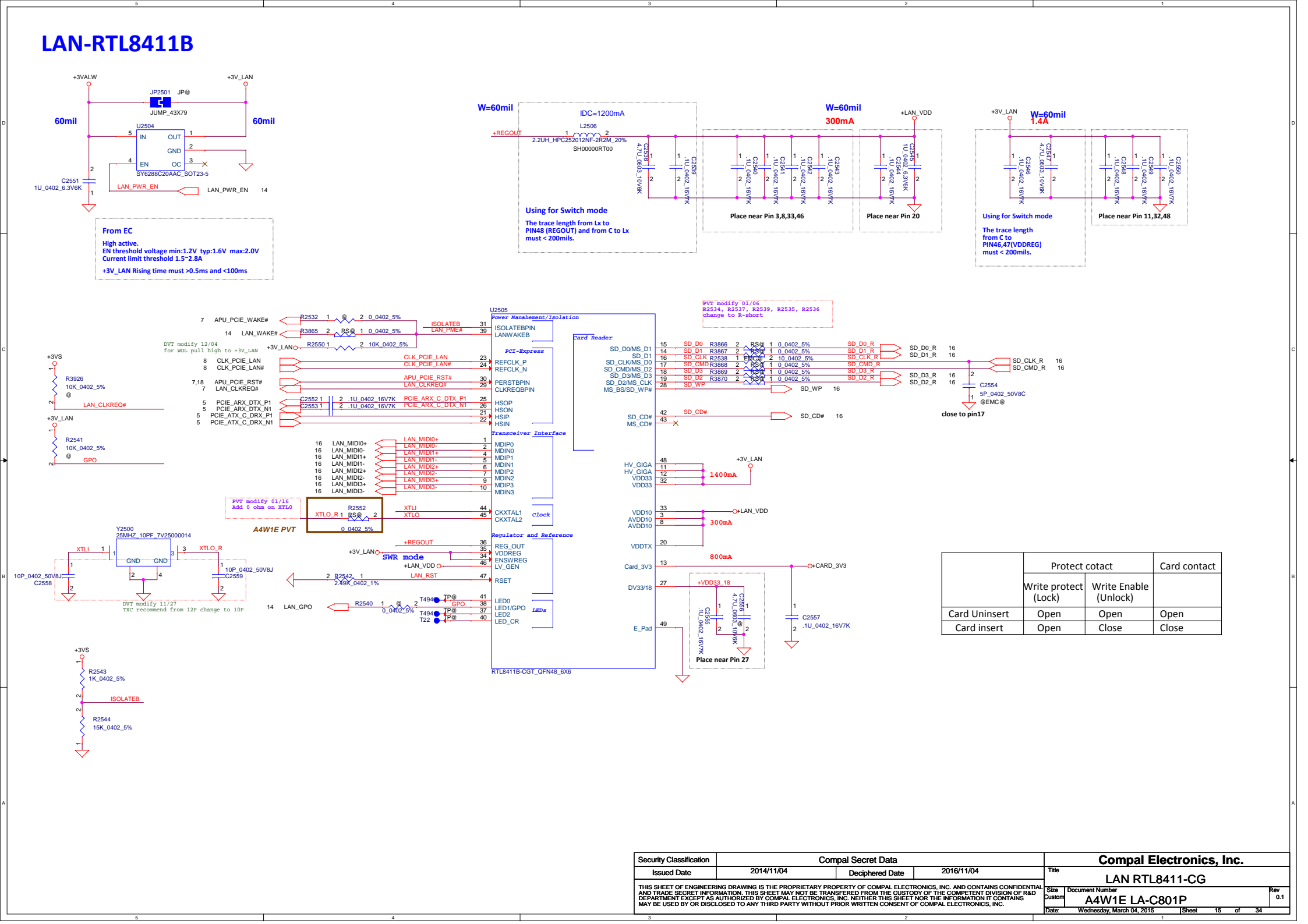
W=60mil

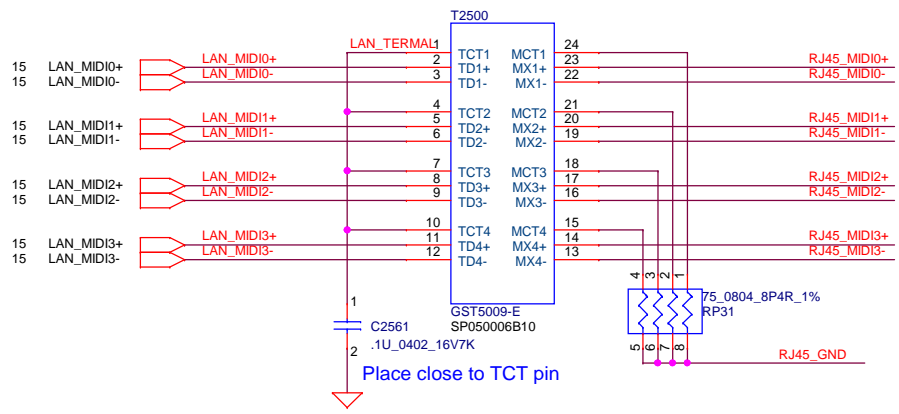
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300mA

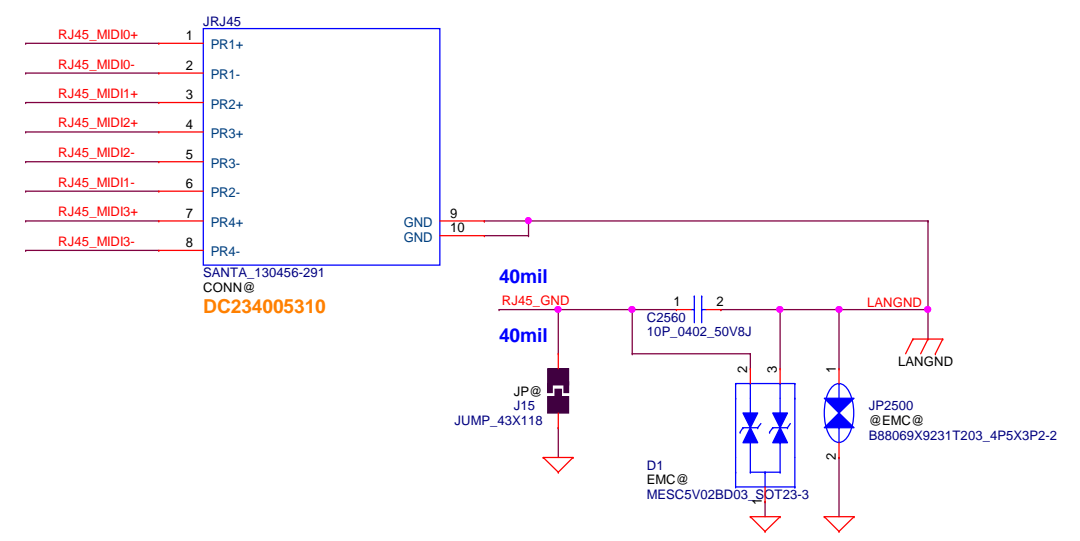
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1.4A

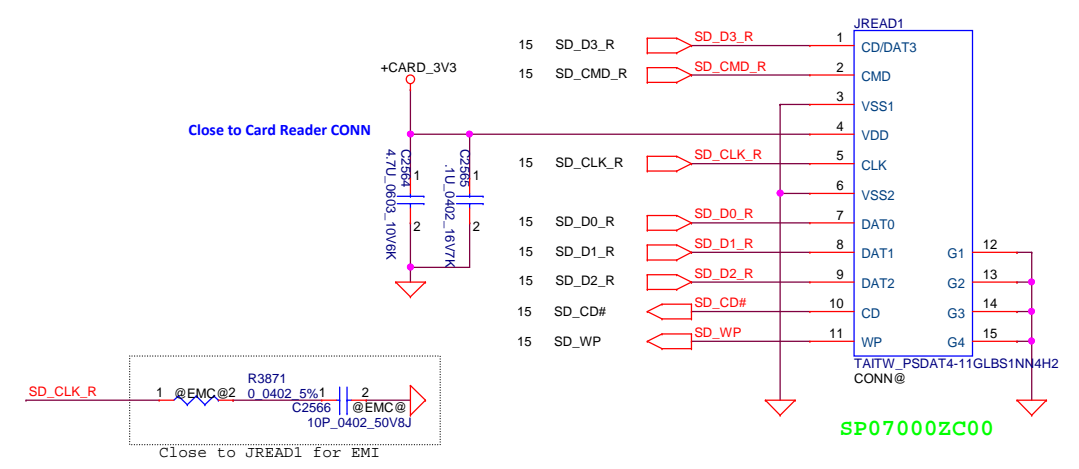
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# LAN Connector

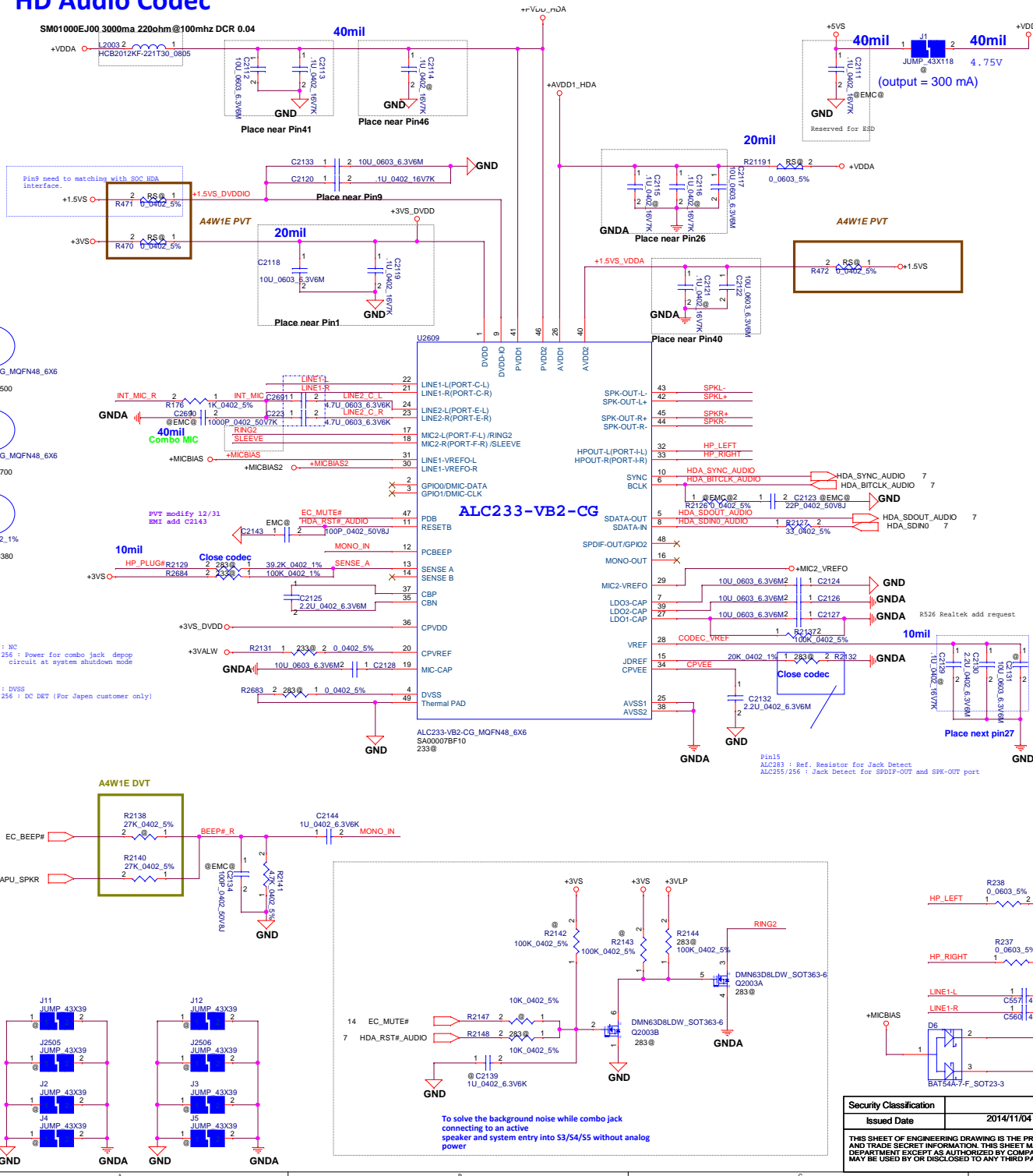


# Card Reader Connector

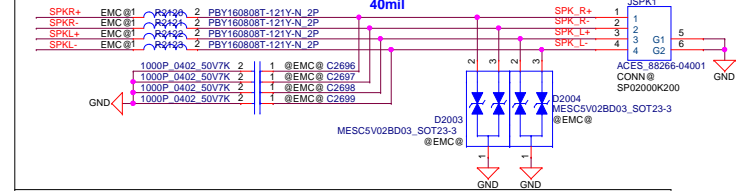


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				Date:	Wednesday, March 04, 2015
				Sheet	16 of 34

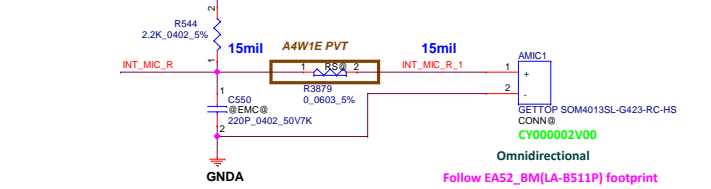
## SM01000EJ00\_3000ma\_220ohm@100mhz DCR 0.04



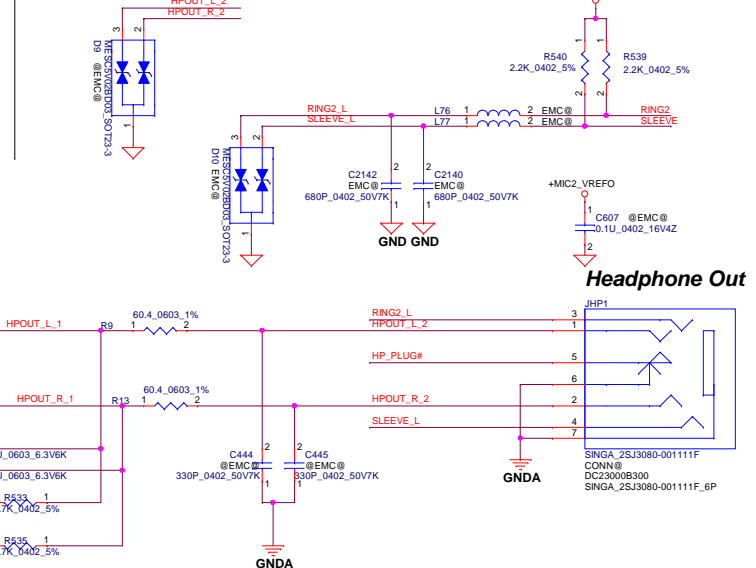
**Int. Speaker Conn.**



### Analog MIC(SMD)



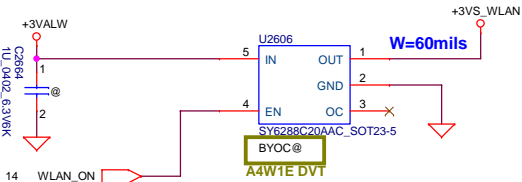
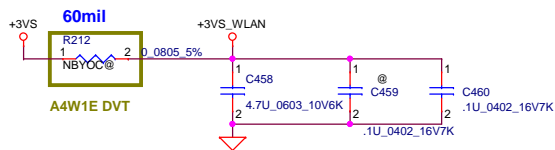
## Headphone Out



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Date:		Wednesday, March 04, 2015				Sheet		17 of 34									

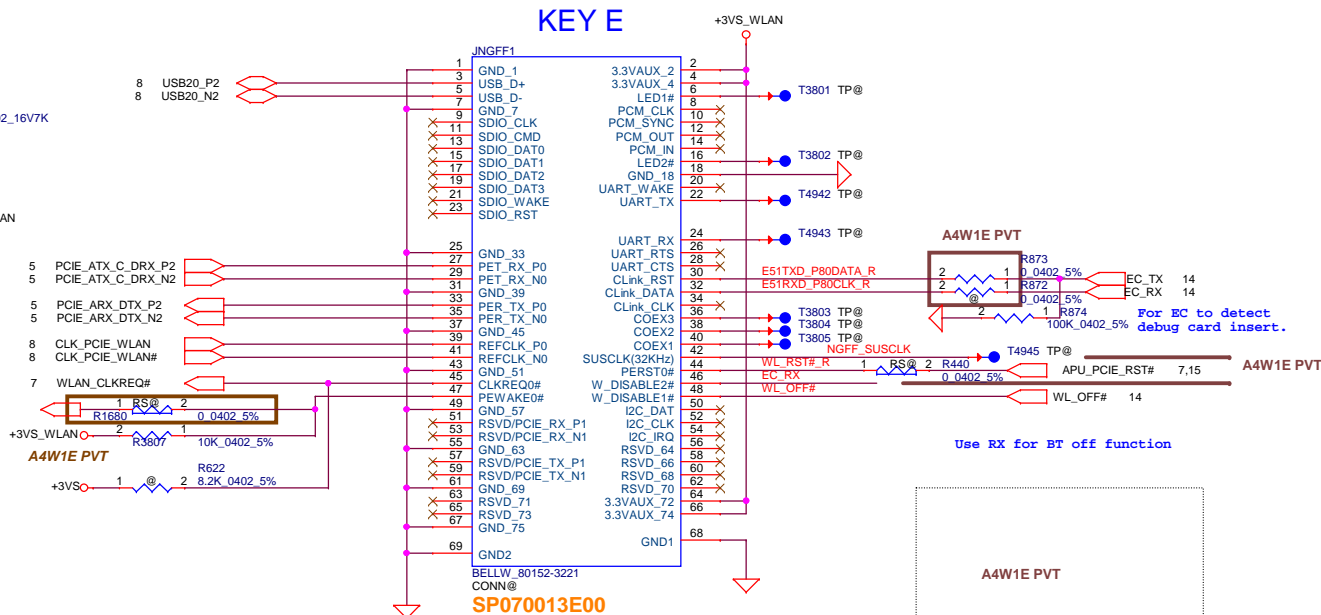
# Wireless LAN

A4W1E



## NGFF WL+BT (KEY E)

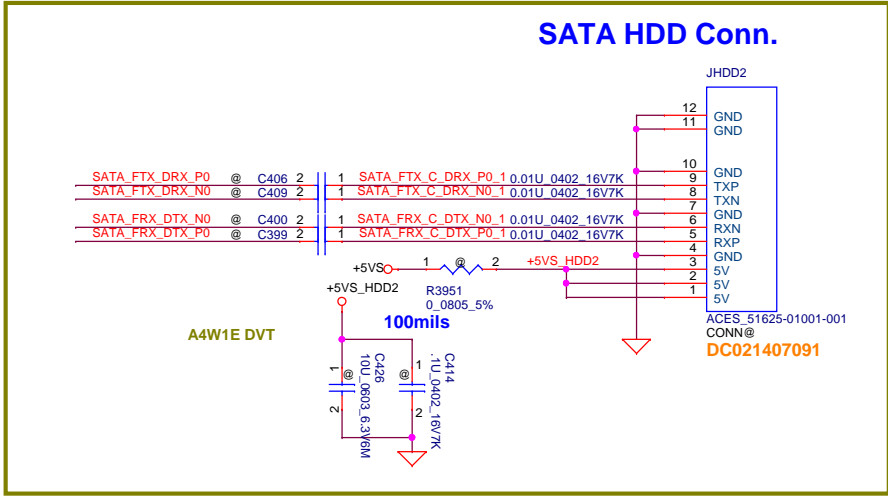
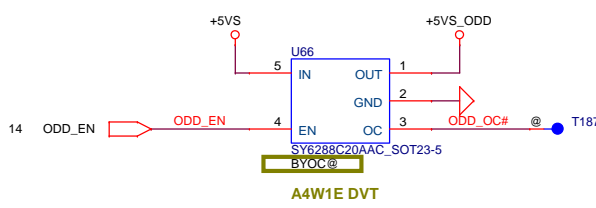
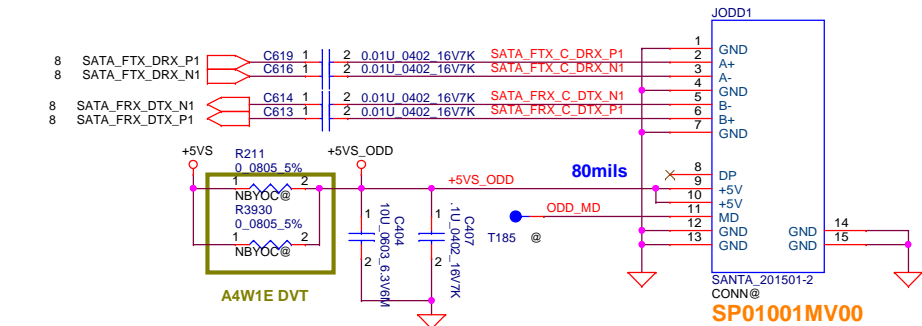
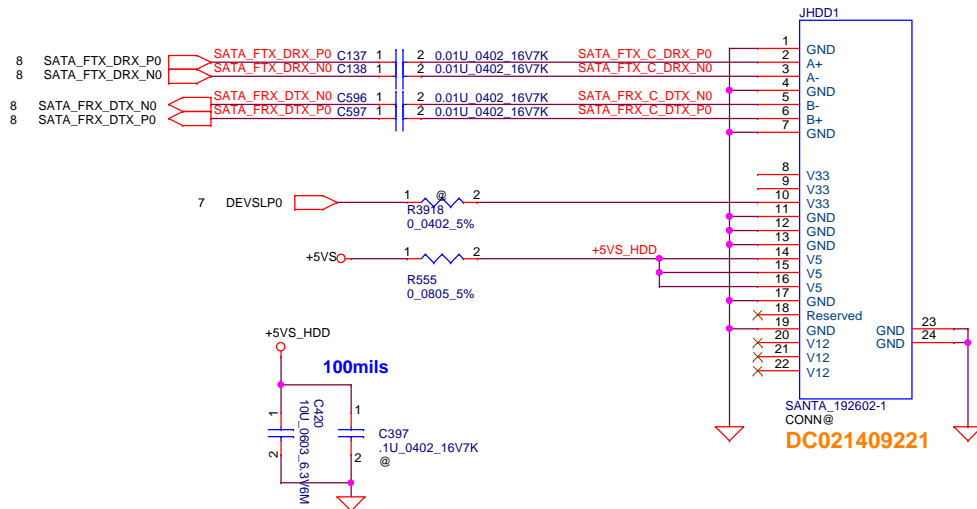
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLK1	73
70	UIM_Power_SBC/GPIO/PWakeup	RESERVED/REFCLK1	71
68	UIM_Power_SBC/GPIO/PWakeup	GND	69
66	UIM_SWP/PERST#	Reserved/PERST	67
64	Reserved	Reserved/PERST	65
62	ALERT# (IO/3.3V)	GND	63
60	IO CLK (IO/3.3V)	Reserved/PERST	61
58	IO CLK (IO/3.3V)	Reserved/PERST	59
56	Wakeup (IO/3.3V)	GND	57
54	Reserved/IO/3.3V	Reserved/IO/3.3V	55
52	Reserved/IO/3.3V	Reserved/IO/3.3V	53
50	Reserved/IO/3.3V	GND	51
48	Reserved/IO/3.3V	REFCLK0	49
46	Reserved/IO/3.3V	REFCLK0	47
44	Reserved/IO/3.3V	GND	45
42	Reserved/IO/3.3V	PERST	43
40	Reserved/IO/3.3V	PERST	41
38	Reserved/IO/3.3V	GND	39
36	Reserved/IO/3.3V	PERST	37
34	Reserved/IO/3.3V	PERST	35
32	Reserved/IO/3.3V	GND	33
30	Reserved/IO/3.3V	PERST	31
28	Reserved/IO/3.3V	PERST	29
26	Reserved/IO/3.3V	PERST	27
24	Reserved/IO/3.3V	PERST	25
22	Reserved/IO/3.3V	PERST	23
20	Reserved/IO/3.3V	PERST	21
18	Reserved/IO/3.3V	PERST	19
16	Reserved/IO/3.3V	PERST	17
14	Reserved/IO/3.3V	PERST	15
12	Reserved/IO/3.3V	PERST	13
10	Reserved/IO/3.3V	PERST	11
8	Reserved/IO/3.3V	PERST	9
6	Reserved/IO/3.3V	PERST	7
4	Reserved/IO/3.3V	PERST	5
2	Reserved/IO/3.3V	PERST	3



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				Rev	0.1
				Date:	Tuesday, March 10, 2015
				Sheet	18 of 34

SATA HDD Conn.

SATA ODD Conn.

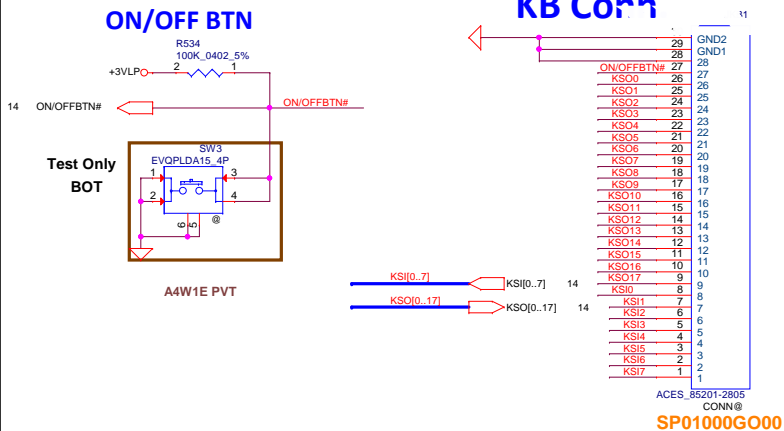


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Date: Wednesday, March 04, 2015		Sheet 19 of 34		0.1	

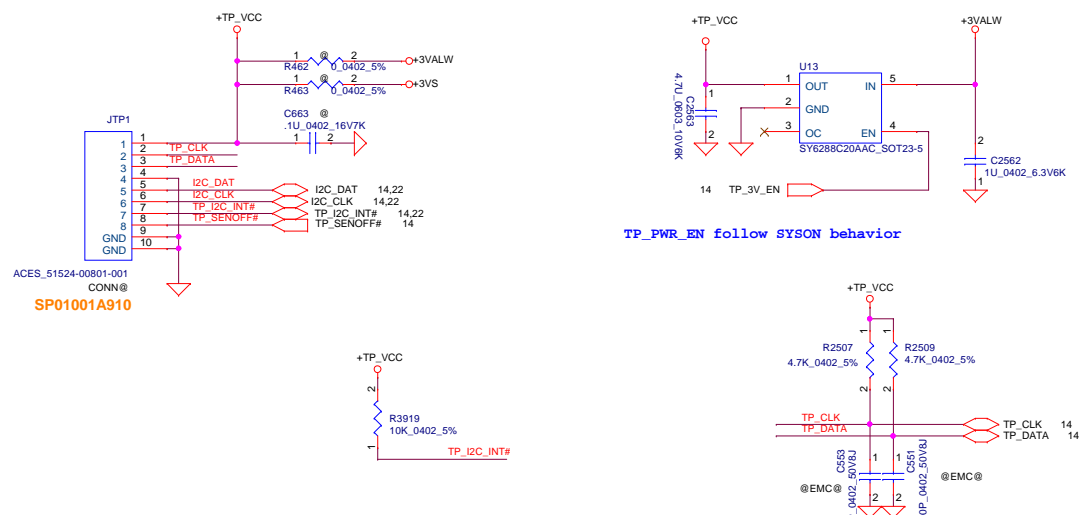




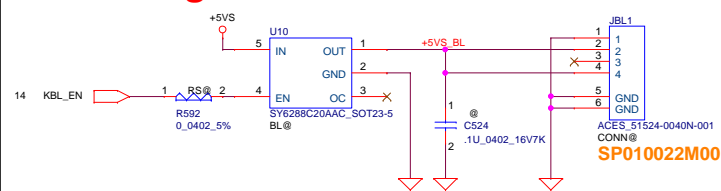
## ON/OFF BTN



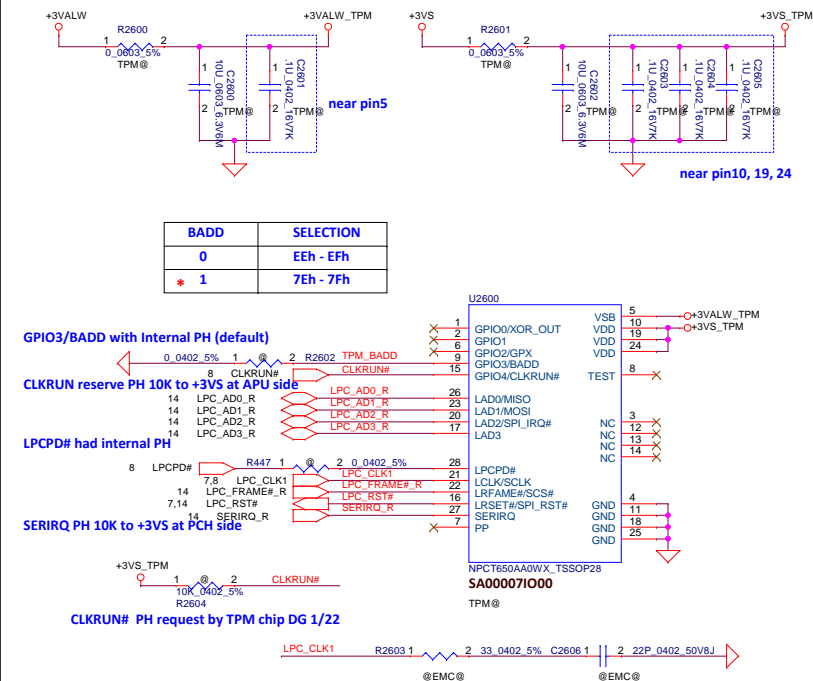
## TP/LED



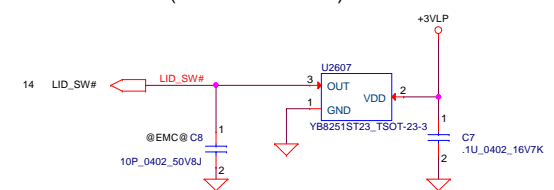
## KB BackLight Conn. Reserve



## TPM Board for 2015



## Lid Switch (Hall Effect Switch)



## LED

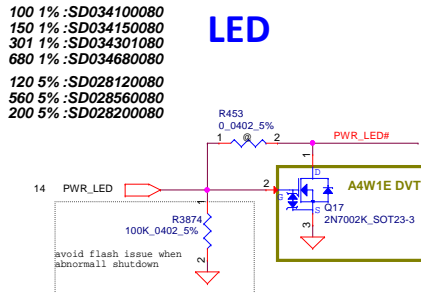
**Dual Amber+Blue**

**LTST-S115TBKF-CA (SC50000C500)**

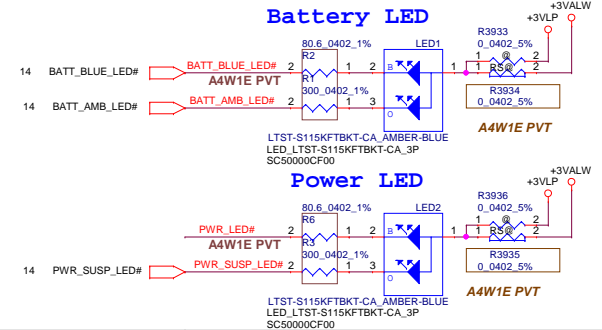
**Vf @ 5 mA :**

**UD5: 1.7 ~ 2.3V**  
(3.3-1.7)/300=5.71 mA  
(3.3-2.3)/300=3.57 mA  
**R min: 100 ohm**  
**R max 700 ohm**

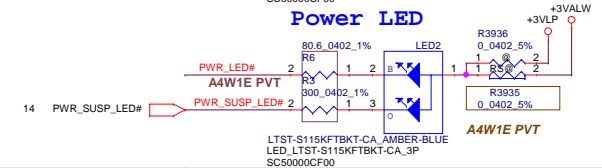
**CB5: 2.65~3.05V**  
(3.3-2.65)/50=13.00 mA  
(3.3-3.05)/100=5.0 mA  
**R min: 50 ohm**  
**R max:475 ohm**



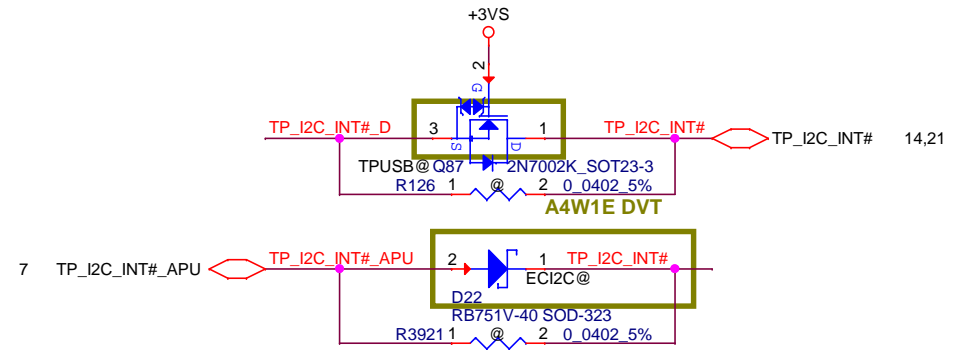
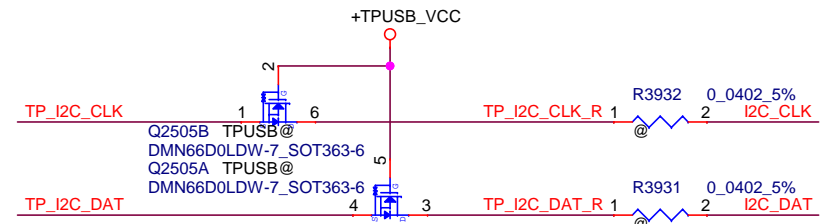
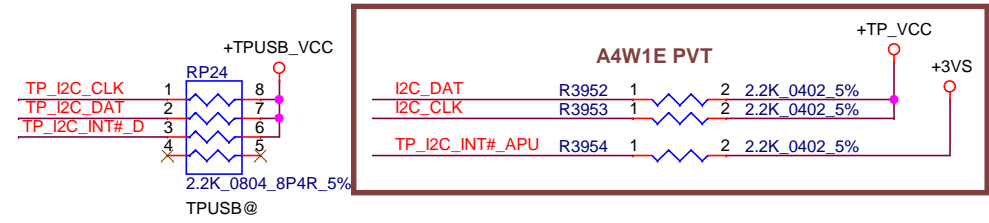
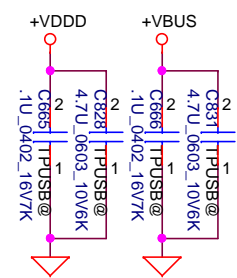
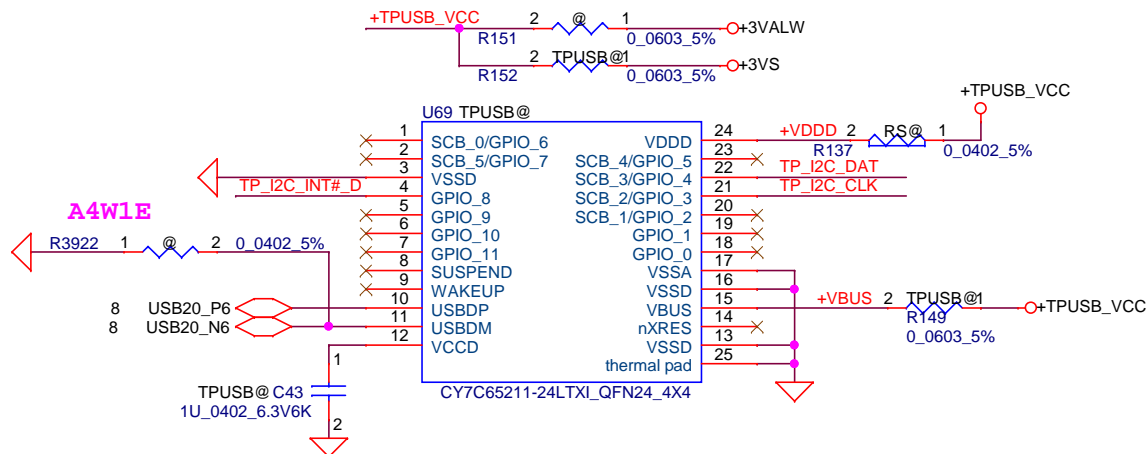
## Battery LED



## Power LED



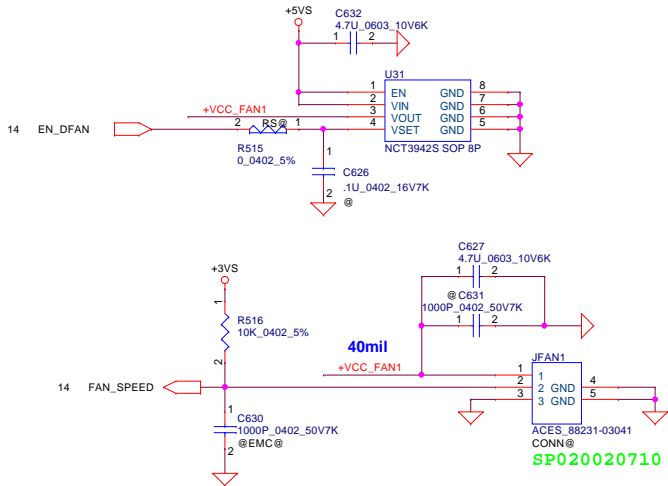
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Issued Date	2014/11/04	Deciphered Date	2016/11/04	KB/TPM/TPM Connector/LED	
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				Custom	0.1
				Document Number	
				A4W1E LA-C801P	
				Date:	Sheet
				Tuesday, March 10, 2015	21 of 34



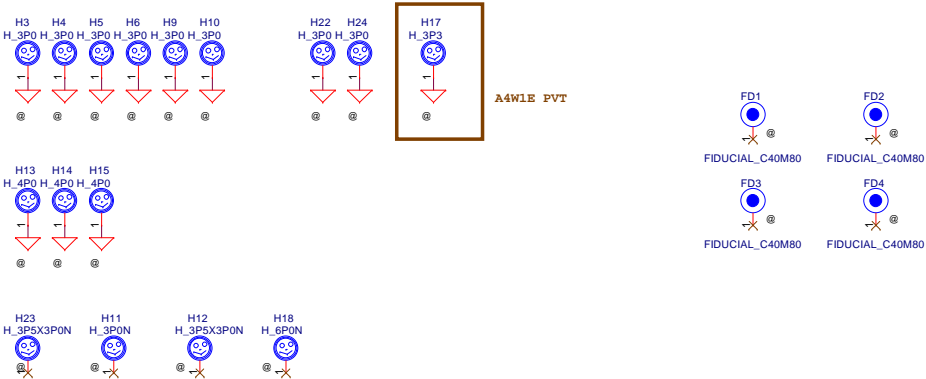
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/11/04	Title	
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Document Number		A4W1E LA-C801P		Rev	
Date:		Wednesday, March 04, 2015		Sheet	
				22 of 34	

FAN1 Conn

FAN Conn

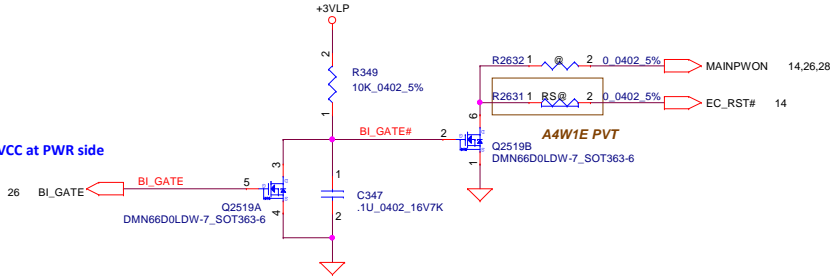


Screw Hole

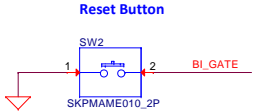


Reset Circuit

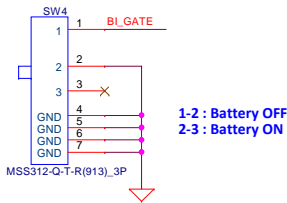
BI\_GATE PH to +RTCVCC at PWR side



Reset Button

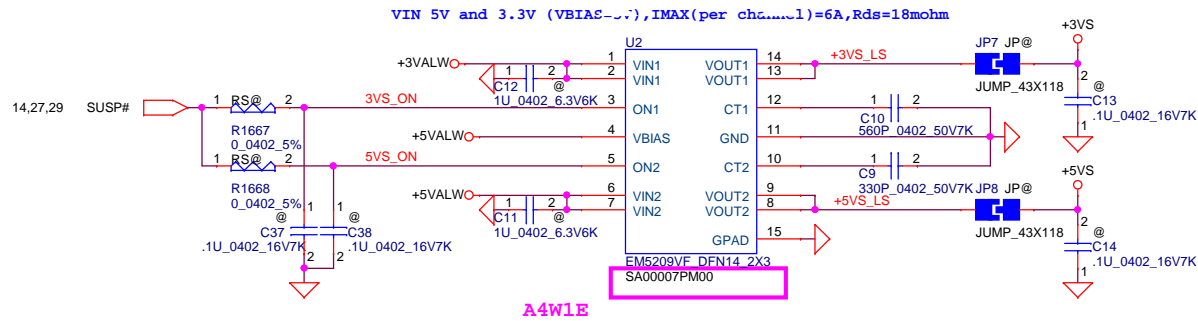


BI SW

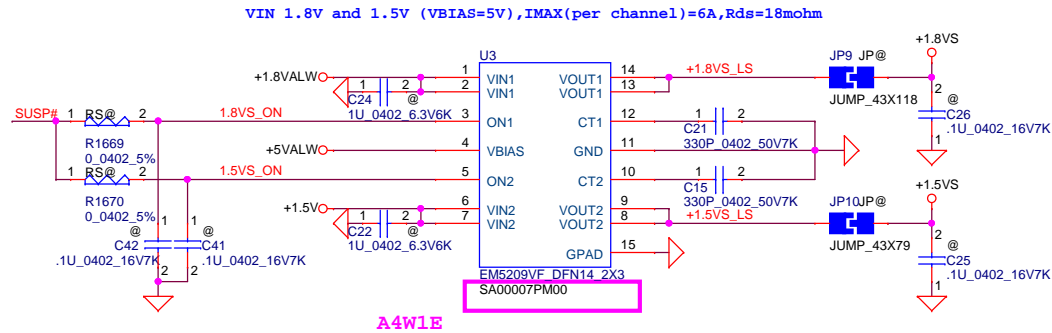


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								Size		Document Number		Rev	
								Custom		A4W1E LA-C801P		0.1	
								Date:		Wednesday, March 04, 2015		Sheet 23 of 34	

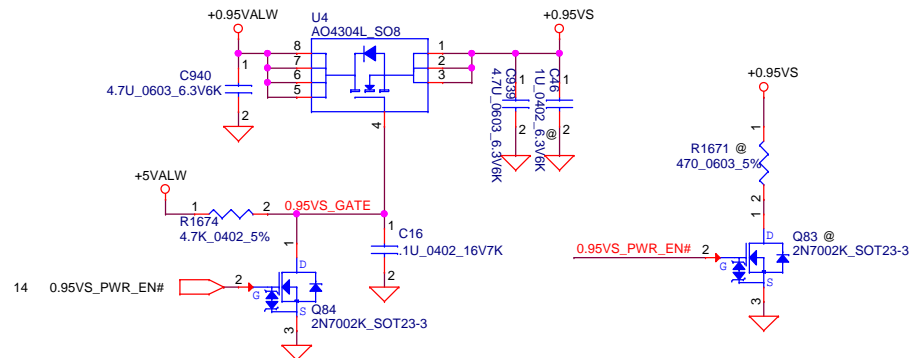
**+5VALW TO +5VS**  
**+3VALW TO +3VS**  
**Load switch**



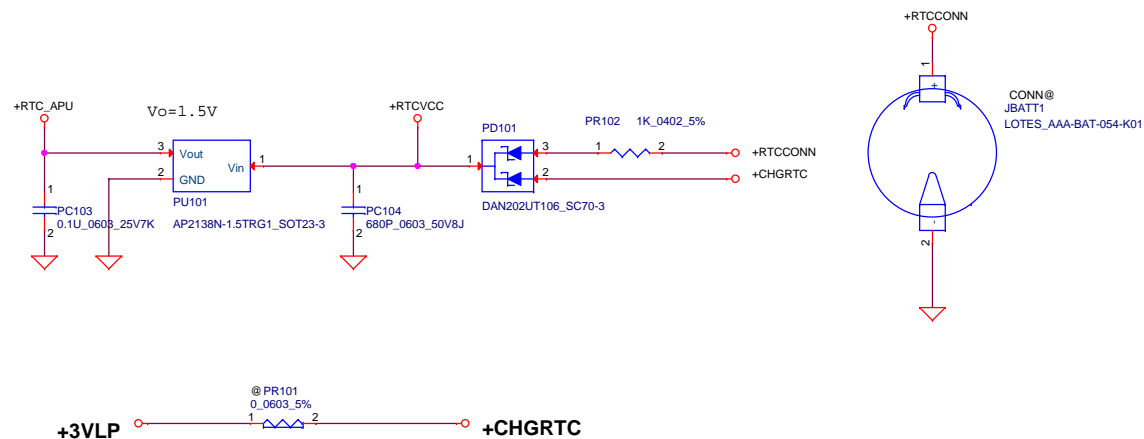
**+1.8VALW TO +1.8VS**  
**+1.5V TO +1.5VS**  
**Load switch**



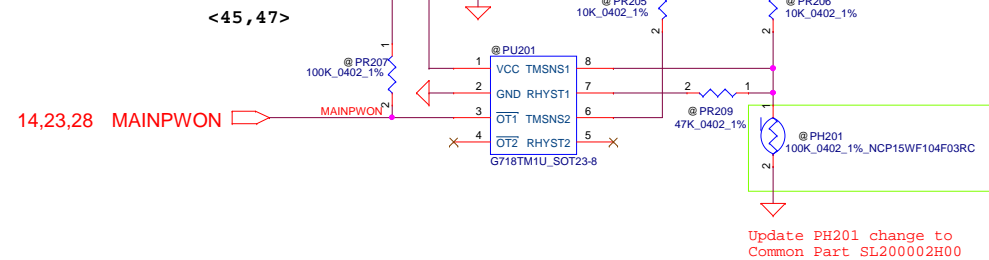
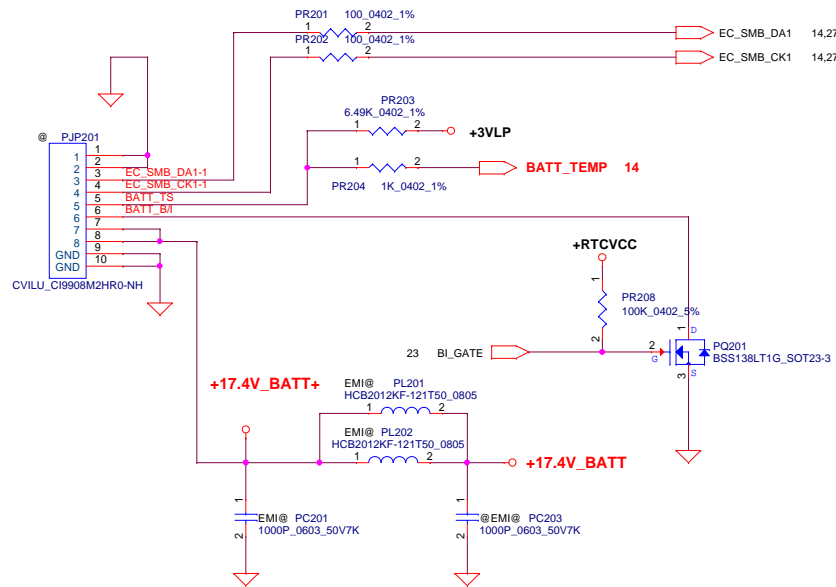
**+0.95VALW to +0.95VS**



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				A4W1E LA-C801P	1.0
Date: Wednesday, March 04, 2015				Sheet	24 of 34



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								Size	Document Number		Rev		
								Custom	A4W1E		0.1		
								Date:		Wednesday, March 04, 2015		Sheet	25 of 34



---Battery\_pin define---  
 PIN1 GND  
 PIN2 GND  
 PIN3 SMD  
 PIN4 SMC  
 PIN5 TS  
 PIN6 B/I  
 PIN7 Batt+  
 PIN8 Batt+  
 ---Battery Con\_pin define---  
 PIN8 GND  
 PIN7 GND  
 PIN6 SMD  
 PIN5 SMC  
 PIN4 TS  
 PIN3 B/I  
 PIN2 Batt+  
 PIN1 Batt+

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.V
PH202(ohm)	7.3K	26.11K

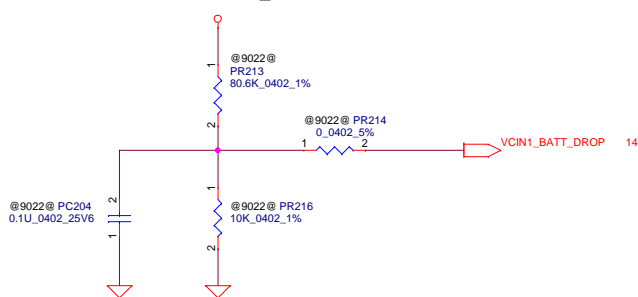
For KB9012 sense 20mΩ	Active	Recovery
45W	48.15W, 0.73V	38.7W, 0.59V
65W	69.55W, 0.73V	55.9W, 0.59V

PH202 under CPU botten side :  
 CPU thermal protection at 92 degree C ( shutdown )  
 Recovery at 56 degree C +EC\_VCCA

2013/10/02  
 Add for ENE9022 Battery Voltage drop detection.  
 Connect to ENE9022 pin64 AD1.

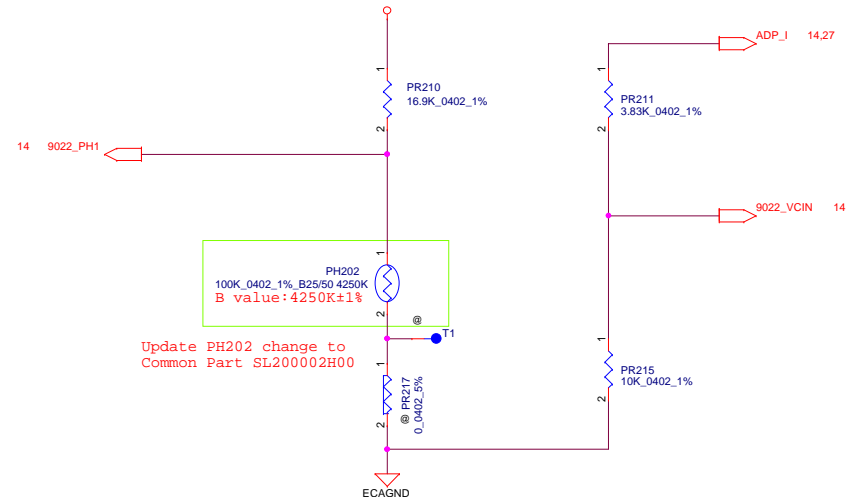
Reserve for 2-cell design

+19VB\_5V



For 45W adapter==>action 48.15W , Recovery 38.7W  
 48.15W:  
 $I_{ada} = 0 \sim 2.253A$  ( $48.15W/19V=2.534A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.534 * 0.02 = 1.01$   
 38.7W:  
 $I_{ada} = 0 \sim 2.036A$  ( $38.7W/19V=2.036A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.036 * 0.02 = 0.814$   
 $CP = 45W * 0.85 = 38.25W$

For 65W adapter==>action 69.55W , Recovery 55.9W  
 69.55W:  
 $I_{ada} = 0 \sim 3.661A$  ( $69.55W/19V=3.661A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 3.661 * 0.02 = 1.464$   
 55.9W:  
 $I_{ada} = 0 \sim 2.942A$  ( $55.9W/19V=2.942A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.942 * 0.02 = 1.177$   
 $CP = 65W * 0.85 = 55.25W$



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								BATTERY CONN / OTP				
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								Date:	Wednesday, March 04, 2015			Sheet

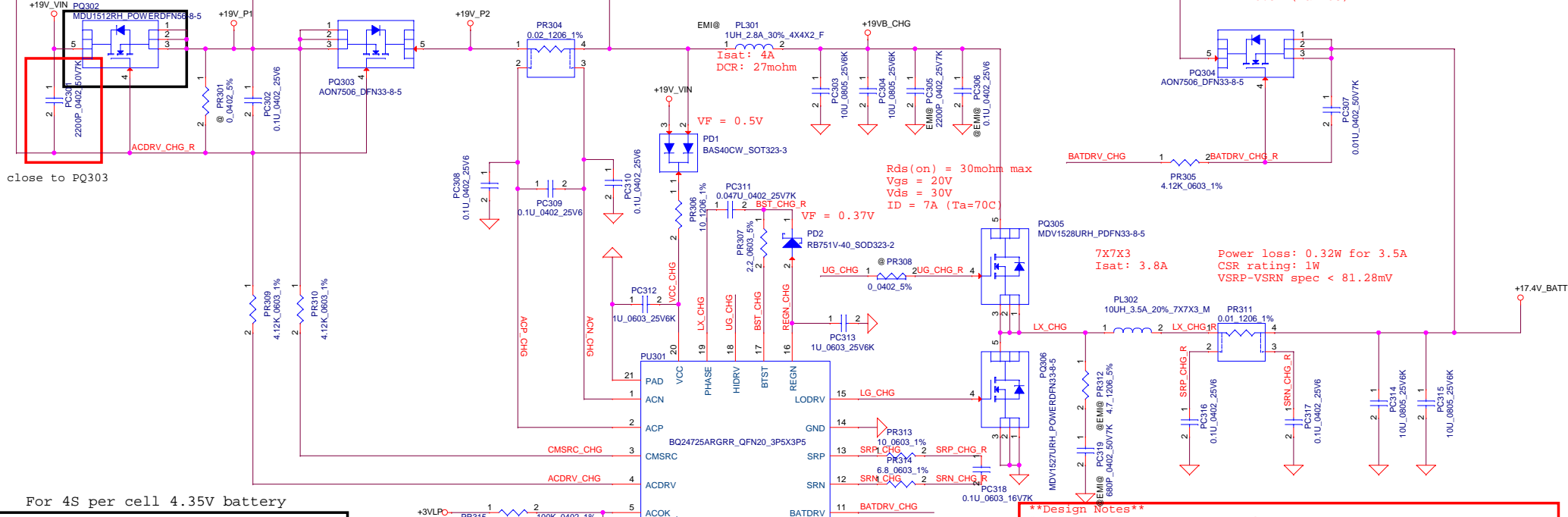


# Protection for reverse input

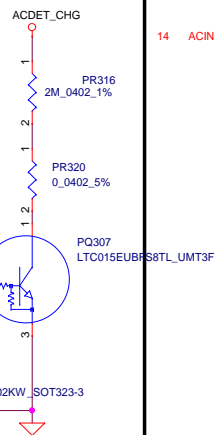
Vgs = 20V  
Vds = 60V  
Id = 250mA

Rds(on) typ=15.8mohm max  
Vgs=20V  
Vds=30V  
ID= 10.5A (Ta=70C)

Need check the SOA for inrush



## For 4S per cell 4.35V battery



Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$$VILIM = 20 * ILIM * Rsr$$

$$ILIM = 3.3 * 100 / (100 + 316) / 20 / 0.01$$

$$= 3.966 A$$

**\*\*Design Notes\*\***

#For 65 /90W system, 3S1P/3S2P battery  
Maximum Charging current 3.5A  
Maximum Battery discharge power 55W.

#Register Setting  
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

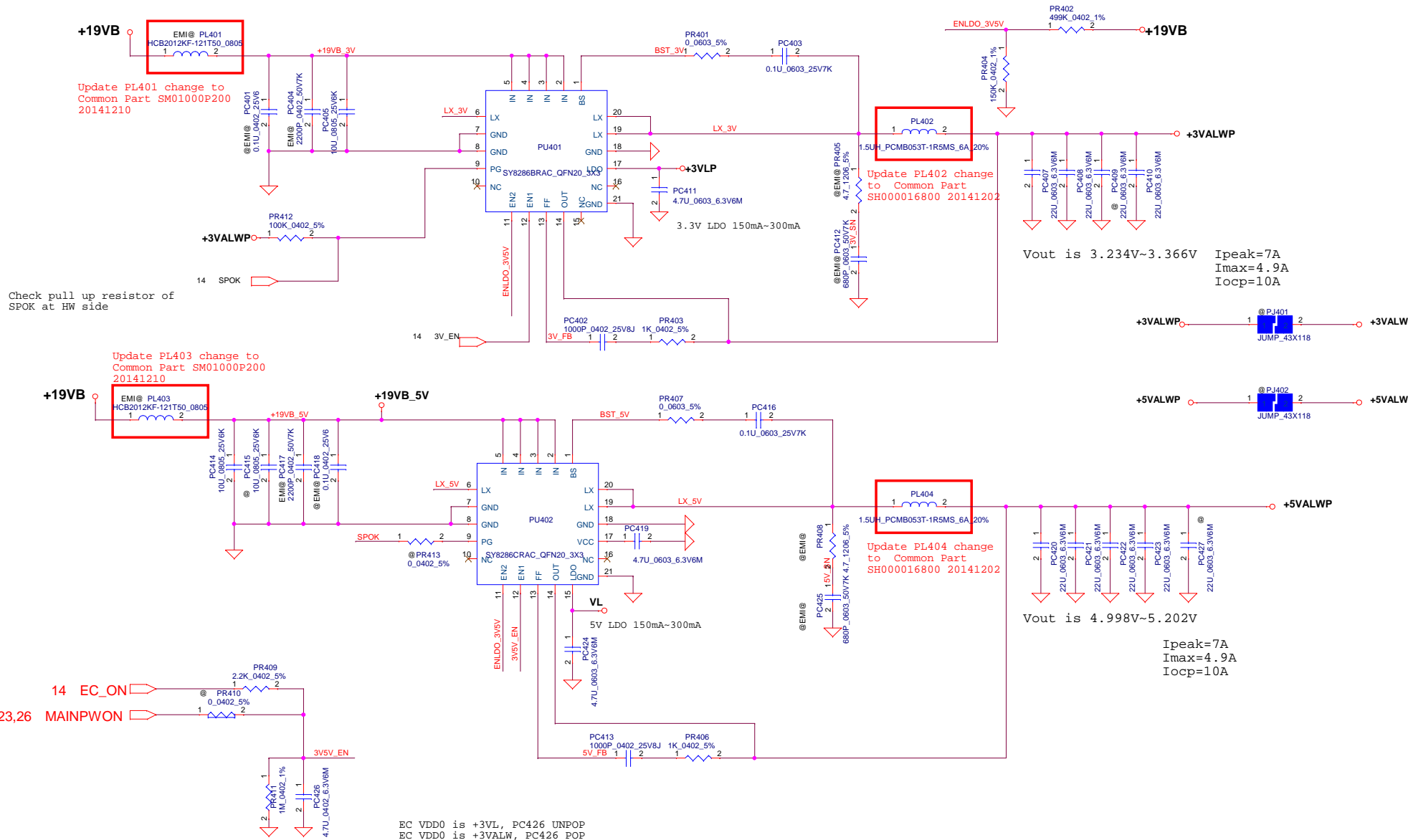
#Circuit Design  
1. ACOK,ILIM pull high voltage need base on 3/5V enable control  
2. Use 10X10 choke and 3X3 H/L Side MOSFET  
Charge current 3.5A  
Power loss : 1.82W  
Power density : 0.81 (15X15)

3. If use 4S per cell 4.35V battery, need additional circuit for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)  
4. PC223 0.22uF can't be changed. (Wrong adapter concern)

5. For the design, need double confirm PQ202,PQ203,PQ204 rating

#Protect function  
1. AC0VP : ACDET voltage > 3.14V  
2. Charger timeout : No communication within 175s(default)  
3. ACOC : 3.33 X Input current DAC setting(default)  
4. CHGOCOP : 3/4.5/6A based on current current setting  
5. BATOVLP : 103-106%  
6. BATLOWV : 2.5V  
7. TSHUT : 155C  
8. IFAULT HI : 750mV (default)  
9. IFAULT LOW : 150mV (default)

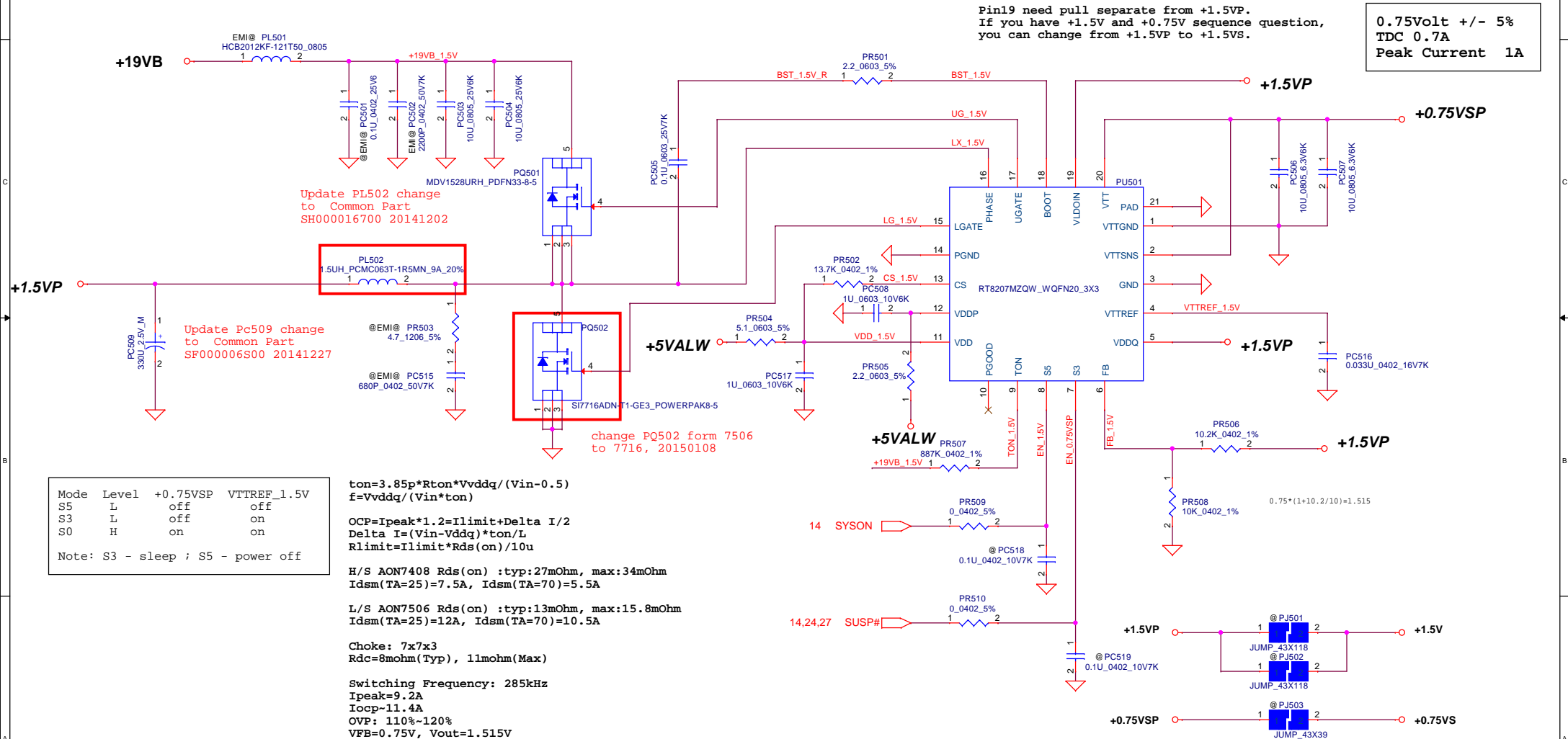
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					Size	Document Number	Rev
					Custom	A4W1E	0.1
Date:		Wednesday, March 04, 2015		Sheet	27	of 34	



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				A4W1E	0.1
				Date: Wednesday, March 04, 2015	Sheet 28 of 34

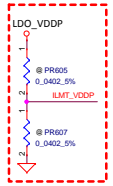
## Module model information

RT8207M\_V1.mdd For Single layer  
RT8207M\_V2.mdd For Dual layer



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								+1.5VP/+0.75VSP	
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						Custom	A4W1E		0.1
						Date:		Wednesday, March 04, 2015	
						Sheet		29 of 34	

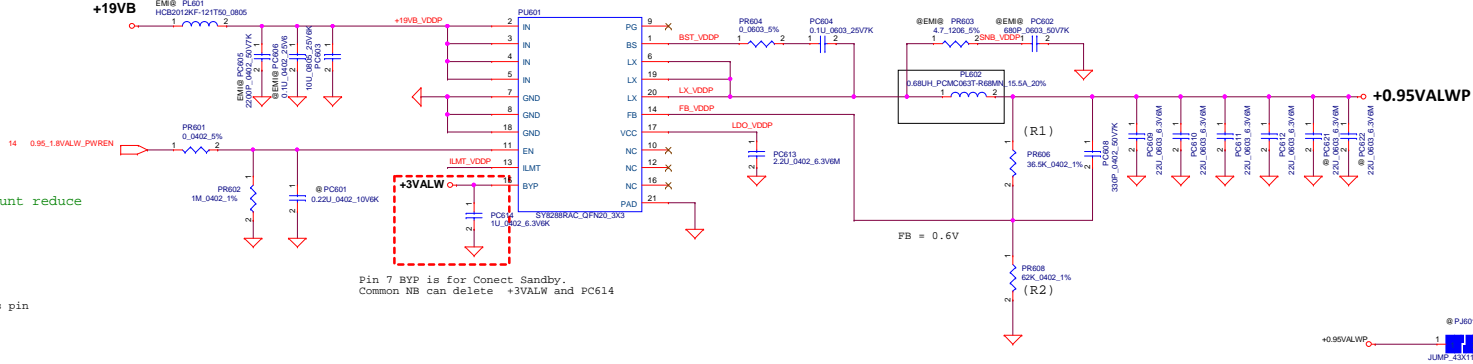
EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



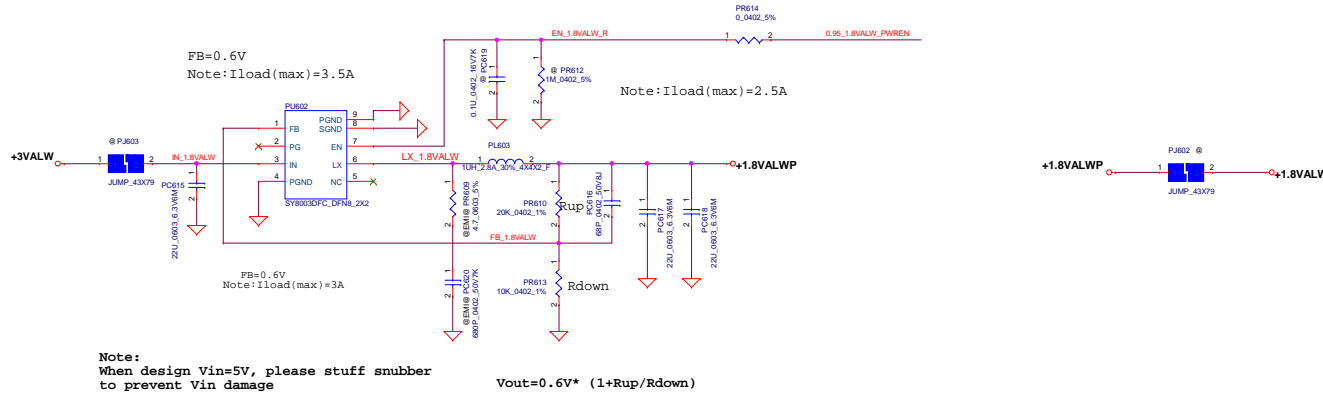
PR606 part count reduce

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

VDDP_ALW_VCTRL	VDDPALW
1	1.062V
0	0.96V



TDC 8A  
VFB=0.6V  
Vout1=0.6V\* (1+R1/R2)=1.062V  
Vout2=0.6V\* (1+R1/(R2+R3))=0.96V

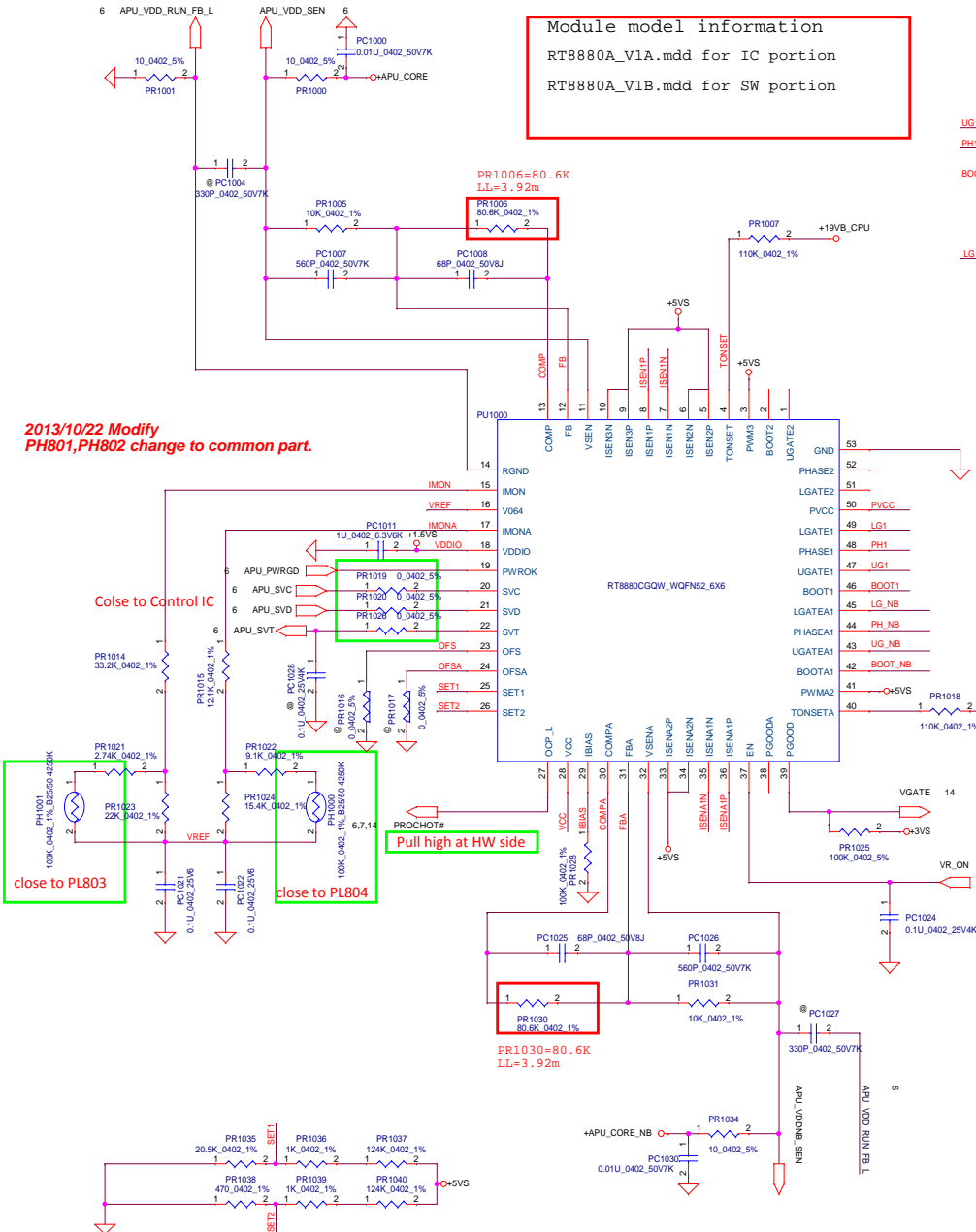


Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

Vout=0.6V\* (1+Rup/Rdown)

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				+0.95VALW/+1.8VALW
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				Date: Wednesday, March 04, 2015 Sheet 30 of 34

2013/10/16 Modify  
PQ801,PQ803 change to AON6552.  
PQ802,PQ804,PQ805 change to AON6554.



2013/10/22 Modify  
PH801,PH802 change to common part.

Close to Control IC

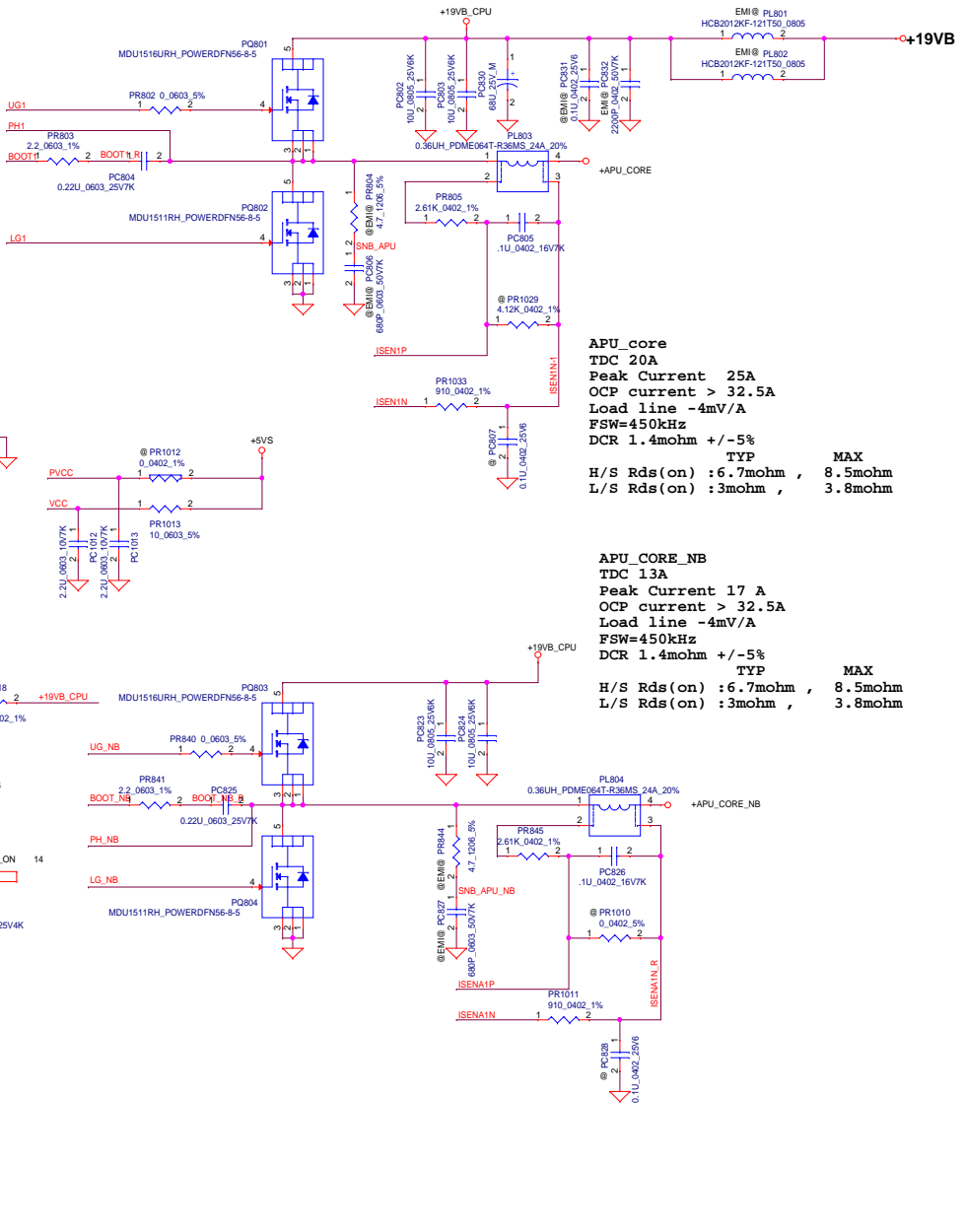
close to PL803

close to PL804

Pull high at HW side

PR1030=80.6K  
LL=3.92m

Delete PR834.PR835.PR836.PR839.PR840.PR841,  
follow vender FAE suggest.  
2013/11/29 modify.



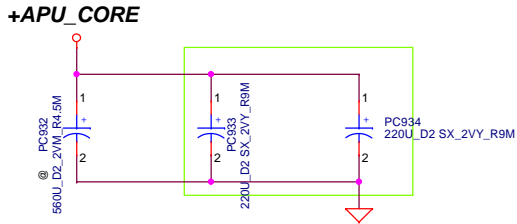
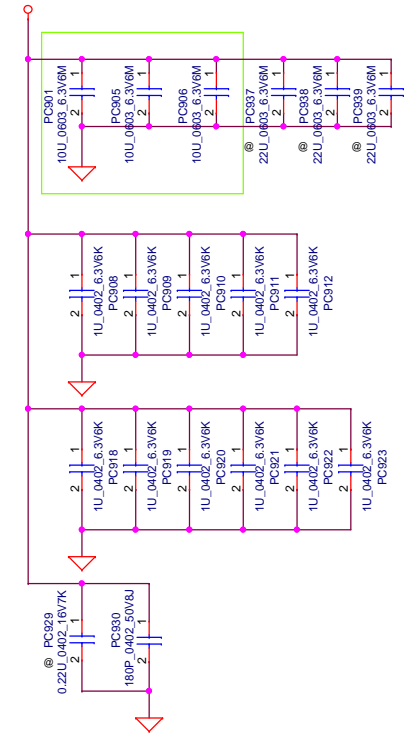
APU\_core  
TDC 20A  
Peak Current 25A  
OCP current > 32.5A  
Load line -4mV/A  
FSW=450kHz  
DCR 1.4mohm +/-5%  
TYP  
H/S Rds(on) : 6.7mohm , 8.5mohm  
L/S Rds(on) : 3mohm , 3.8mohm

APU\_CORE\_NB  
TDC 13A  
Peak Current 17 A  
OCP current > 32.5A  
Load line -4mV/A  
FSW=450kHz  
DCR 1.4mohm +/-5%  
TYP  
H/S Rds(on) : 6.7mohm , 8.5mohm  
L/S Rds(on) : 3mohm , 3.8mohm

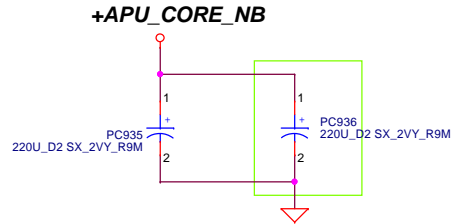
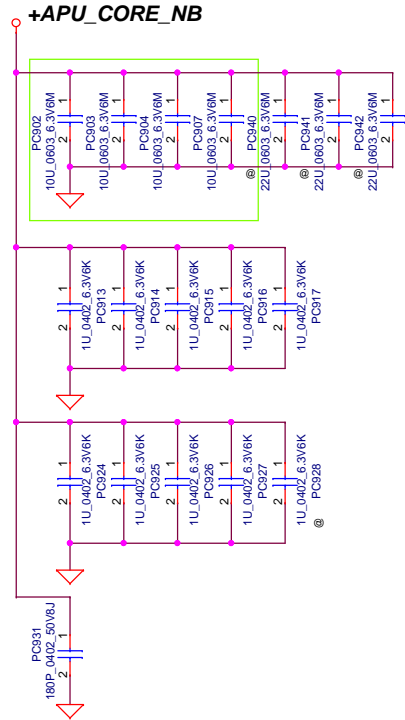
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Issued Date		Deciphered Date		Title	
2012/06/19		2012/07/31		CPU CORE	
Size		Document Number		Rev	
Custom		A4W1E		1A	
Date		Wednesday, March 04, 2015		Sheet	
				31 of 34	

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# +APU\_CORE (36.4)



# +APU\_CORE\_NB (36.5)



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						Date:	Wednesday, March 04, 2015		Sheet	32	of



Page 1 of 1  
for PWR

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				Custom A4W1E	0.1
Date:	Wednesday, March 04, 2015	Sheet	33	of	34

Item	Page	Date	Reason for change	Phase
01	06	2015/01/05	For AMD Beema and Kabini APU colay	DVT
02	14	2015/01/05	Board ID update from 0 to 1	
03	19	2015/01/05	HDD connector too close to speaker	
04	07	2015/01/12	Power leakage when S3/S4/S5	
05	13	2015/01/19	HDMI test	
06	14	2015/01/19	For AMD Beema and Kabini APU colay	
07	21	2015/01/23	Layout PCB footprint correct	
08	11	2015/01/27	BOM update for DDR 1.5V power	
09	12,20	2015/01/27	BOM update as source request (SM070003K00->X1)	
10	17	2015/01/27	PC Beep issue on DOS mode	
11	21,22	2015/01/27	BOM update to Main source	
12	14	2015/01/27	BOM update to Main source	
13	18	2015/01/27	BOM structure update for BYOC/NBYOC	
14	19	2015/01/27	BOM structure update for BYOC/NBYOC	
15	14	2015/02/25	Board ID update from 1 to 2	PVT
16	22	2015/02/25	Debug convenience	
17	18	2015/02/25	Intel WLAN module request(pin 32 & 46 disconnect)	
18	18	2015/02/25	Remove un-used net from WLAN	
19	08	2015/02/25	48MHz crystal tolerance fine tune	
20	07	2015/02/25	To identify project(14" & 15")	
21	07	2015/02/25	To identify platform(Beema/Kabini)	
22	21	2015/02/25	LED brightness test result	
23	23	2015/03/01	ME drawing update	
24		2015/03/04	Part count request	
25	21	2015/03/10	Unstuff un-used component for PCB R1.0	
26	14	2015/03/30	Board ID update from 2 to 3	Pre MP
27	04	2015/03/30	PCB part number update to 1A	

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